IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC.,	)	
Plaintiffs,	)	C.A. No. 21-1453 (RGA)
v.	)	
NETLIST, INC.,	)	
Defendant.	)	

NOTICE OF SUPPLEMENTAL AUTHORITY IN SUPPORT OF PLAINTIFFS' OPPOSITION TO NETLIST'S MOTION TO DISMISS PLAINTIFFS' FIRST AMENDED COMPLAINT

Pursuant to D. Del. LR 7.1.2(b), Plaintiffs Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. (collectively, "Samsung") submit this notice of supplemental authority in support of Samsung's opposition (D.I. 27) to Netlist's motion to dismiss Samsung's first amended complaint.

First, in the patent infringement action between Netlist and Google pending in the Northern District of California, the court granted Google's motion for leave to amend its answer and counterclaims to, *inter alia*, add a defense that the '912 patent is unenforceable due to inequitable conduct. *See* Exhibit A, *Netlist, Inc. v. Google LLC*, No. 09-cv-5718, D.I. 258 (N.D. Cal. May 5, 2022). Google's inequitable conduct defense is based on the same misrepresentations as Samsung's claim that the '912 patent is unenforceable due to inequitable conduct and unclean hands. *Compare Netlist, Inc. v. Google LLC*, No. 09-cv-5718, D.I. 206-2 at 4–10 (N.D. Cal. Sept. 17, 2021) *with* D.I. 14, ¶¶ 370–403. In granting Google's motion, the court rejected Netlist's argument that the defense failed because the statements at issue purportedly constituted

permissible attorney argument before the Patent Office. Ex. A at 39-40. In the present action, Netlist made the same argument in support of its motion to dismiss Samsung's claim that the '912 patent is unenforceable. *See* D.I. 25 at 18. Netlist's motion to dismiss Samsung's claim should be denied for the reasons set forth in Samsung's opposition (D.I. 27) to Netlist's motion and in the order issued by the Northern District of California.

Second, the Patent Trial and Appeal Board ("PTAB") recently issued a Decision Granting Institution of *Inter Partes* Review of U.S. Patent No. 10,217,523 (the "Institution Decision"). *See* Exhibit B, IPR2022-00063, Paper No. 13 (May 5, 2022). In the Institution Decision, the PTAB determined that Samsung demonstrated a reasonable likelihood of prevailing on multiple grounds of unpatentability, including its assertion that claims 1-34 of the '523 patent would have been obvious over the combination of Ellsberry and Jeddeloh752. *See id*. at 16-47. The Institution Decision is relevant to Netlist's motion to dismiss Samsung's claim that the '523 patent is unenforceable due to inequitable conduct and unclean hands based on the failure to disclose Ellsberry and Jeddeloh752 to the Patent Office during prosecution of the '523 patent. *See* D.I. 25 at 18-19. In the motion, Netlist argues that Samsung failed to adequately plead that Ellsberry and Jeddeloh752 are "but-for" material to the patentability of the '523 patent. *See id.* The Institution Decision provides further support for Samsung's allegations that Ellsberry and Jeddeloh752 are material and not cumulative of other art or information that was before the Patent Office, and that the Patent Office would not have allowed one or more claims of the '523 patent to issue had it been aware of Ellsberry and Jeddeloh752. *See* D.I. 27 at 17–18.

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EXHIBIT A

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

NETLIST, INC.,

Plaintiff,

vs.

GOOGLE LLC,

Defendant.

AND RELATED COUNTERCLAIM.

Case No: 4:09-cv-05718 RS

ORDER ON GOOGLE'S MOTION TO STRIKE, GOOGLE AND NETLIST'S RESPECTIVE MOTIONS FOR SUMMARY JUDGMENT, AND GOOGLE'S MOTION TO AMEND

I. INTRODUCTION

Netlist brings the instant action against Google for infringement of U.S. Patent No. 7,619,912 ("the '912 patent"). The '912 patent relates to memory module technology. A memory module (also known as a "dual in-line memory module" or "DIMM") contains individual memory devices (e.g., "dynamic random-access memory" or "DRAM") arranged on a printed circuit board. The memory devices are combined into sets or "ranks" to increase the capacity of the module. For a given amount of total module memory, it is more cost-effective to use a larger number of low-density memory devices, rather than a smaller number of high-density memory devices. However, most computer systems are unable to take advantage of this feature. The '912 patent overcomes this issue by, among other things, implementing circuitry into the memory module that translates between the computer system's memory controller and the memory devices on the module.

Presently pending are: (1) Google's Motion to Strike Netlist's New Assertion of Claim 16 and New Dates for Priority and Conception that Were Not in Its Original Patent Local Rule

3-1 Disclosures, Dkt. 153; (2) Google's Motion for Summary Judgment on the Issue of Absolute Intervening Rights, Dkt. 155; (3) Netlist's Motion for Partial Summary Judgment on Google's Intervening Rights Defense for Claim 16, Dkt. 156; and (4) Google's Motion to Amend Answer and Counterclaims, Dkt. 206. Google's motion to strike is granted with respect to the new priority and conception dates for lack of diligence; the motion is denied as to claim 16, on the ground that Netlist could not have asserted the claim earlier. With regard to the defense of intervening rights, Netlist's motion for summary judgment as to claim 16 is granted because the reexamined claim—confirmed to be patentable as originally issued and rewritten in independent form—is identical to the original claim 16. Google's motion for summary judgment on its defense of intervening rights is denied as to claim 16; the motion is granted as to the remainder of Netlist's asserted claims, which were narrowed during the reexamination proceedings. Finally, Google's motion to amend its Answer and Counterclaims is granted on the ground that good cause has been shown and the liberal standard of Federal Rule of Civil Procedure 15(a)(2) has been met.

II. MOTION TO STRIKE

A. RELEVANT BACKGROUND

Netlist filed a Complaint for Patent Infringement on December 4, 2009. Dkt. 1. On April 8, 2010, Netlist served its Disclosure of Asserted Claims and Infringement Contentions in accordance with Patent Local Rule ("PLR") 3-1. Dkt. 152-6. The disclosure identified claims 1, 3, 4, 6-11, 15, 18-22, 24, 25, 27-29, 31-34, 36-39, 41-45, and 50 of the '912 patent, and asserted the claims against certain memory modules known as 4-Rank DDR2 FBDIMMs. Id. at 1-2. Claim 16 of the '912 patent was not asserted. Id. Netlist further asserted that the '912 patent is entitled to a priority date of July 1, 2005. Id.

On October 21, 2010, Google filed a request for *inter partes* reexamination of the '912 patent, challenging each of the 34 claims asserted by Netlist. Dkt. 153-6. The PTO granted Google's request on January 18, 2011, and this action was stayed pending completion of the reexamination proceedings on January 26, 2011. Dkt. 68. On February 25, 2011, the PTO *sua*

sponte consolidated Google's reexamination proceeding with proceedings initiated by Inphi Corporation ("Inphi") and Smart Modular Technologies Inc. ("SMT"). Dkt. 153-8.

The reexamination proceedings and resulting appeal lasted more than a decade. During those proceedings, the Patent Trial & Appeal Board ("PTAB") invalided nearly all of the original claims of the '912 patent based on a combination of prior art references called Amidi and Dell-2. As a result, Netlist canceled or amended each of the 34 claims it had asserted against Google in this action. Claim 16—which was not asserted against, or challenged by, Google but was challenged by Inphi—was confirmed. The Patent and Trademark Office ("PTO") issued a reexamination certification on February 8, 2021, and this case reopened on February 17, 2021. Dkt. 111.

On March 4, 2021, the parties filed a Joint Case Management Conference Statement, wherein they recognized that the reexamination proceedings may gave rise to a defense of intervening rights and requested early resolution of the issue. Dkt. 115 at 3. Given that the memory modules used by Google likely changed during the pendency of the stay, the parties proposed that Netlist take targeted discovery to identify the memory modules currently in use and then serve "amended infringement contentions," after which they would brief the issue of intervening rights. Id. at 3-4, 5. The parties' proposal was adopted and the deadline for Netlist to serve "amended infringement contentions" was set for June 18, 2021. Dkt. 117.

Thereafter, Netlist sought discovery from Google to identify the memory modules currently in use. On May 19, 2021, Google served discovery responses, wherein it first disclosed its use of DDR4 DIMMs. Dkt. 169-11.[1] In the meantime, Netlist decided to serve amended claim charts on a rolling basis. Dkt. 169-9. On May 19, 2021, Netlist served a claim chart asserting infringement of claim 16. Id. Netlist then served its Amended Disclosure of Asserted Claims and Infringement Contentions on June 18, 2021. Dkt. 152-8. The amended

[1] The memory module technology at issue ("double data rate" or "DDR" technology) is subject to standards promulgated by the Joint Electron Devices Engineering Counsel ("JEDEC"). At the time this action was stayed, Google was using second and third generation (i.e., DDR2 and DDR3) memory modules. In September 2012, JEDEC issued the DDR4 standard. Dkt. 170-6. Google began using DDR4 standard technology sometime in 2014.

disclosure asserts claim 16 and identifies the accused instrumentalities as certain memory modules compliant with the DDR4 standard. Id. at 1-2. The amended disclosure also asserts a priority date "as early as March 5, 2004" and a conception date of "no later than mid-2003." Id. at 6. Netlist cites the deposition of a named inventor, Jayesh Bhakta, which took place on September 17, 2010, to support these new dates. Id.

B. LEGAL STANDARD

Patent Local Rule 3-1 requires that a party claiming patent infringement serve a "Disclosure of Asserted Claims and Infringement Contentions" within 14 days of the initial case management conference. Rule 3-1 includes subparts requiring, *inter alia*, the disclosure of each claim of the patent allegedly infringed; for each claim alleged, specific infringement contentions; and the priority date to which each claim is entitled. See also O2 Micro Int'l, Ltd. v. Monolithic Power Sys., Inc., 467 F.3d 1355, 1359 (Fed. Cir. 2006) (the local patent rules "require parties to state early in the litigation and with specificity their contentions with respect to infringement and invalidity"). The purpose of these rules "is to ensure early crystallization of the parties' theories, and specifically, to place the burden on the plaintiff to quickly decide on and disclose the contours of its case." OpenTV, Inc. v. Apple, Inc., No. 15-CV-02008-EJD (NC), 2016 WL 3196643, at *3 (N.D. Cal. June 9, 2016).

The Patent Local Rules seek to "balance the right to develop new information in discovery with the need for certainty as to the legal theories." O2 Micro, 467 F.3d at 1366. Accordingly, amendment of infringement contentions "may be made only by order of the Court upon a timely showing of good cause." PLR 3-6; see also O2 Micro, 467 F.3d at 1366 (affirming validity of patent rule that requires early disclosure of infringement contentions and good cause to amend the same); Verinata Health, Inc. v. Ariosa Diagnostics, Inc., 236 F. Supp. 3d 110, 1113 (N.D. Cal. 2017) (noting that, in contrast to the more liberal standard for amending pleadings, the standard to amend claim charts is decidedly conservative, and designed to prevent the "shifting sands" approach to claim construction). "In determining whether good cause exists, courts consider (1) whether the moving party was diligent in moving to amend its contentions and (2) whether the non-moving party would suffer prejudice

if leave to amend were granted." Koninklijke Philips N.V. v. Acer Inc., No. 18-CV-01885-HSG, 2019 WL 652868, at *1 (N.D. Cal. Feb. 15, 2019).

The party moving to amend bears the burden of demonstrating diligence, both in discovering the basis for the amendment and in seeking leave to amend once that basis has been discovered. Verinata Health, 236 F. Supp. 3d at 1113. If the moving party satisfies its burden, the Court must then consider prejudice to the opposing party in determining whether to grant leave to amend. Advanced Micro Devices, Inc. v. LG Elecs., Inc., No. 14-CV-01012-SI, 2017 WL 732896, at *2 (N.D. Cal. Feb. 24, 2017). Prejudice is typically found when amendment stands to disrupt the case schedule or other court orders. Id. (citing Karl Storz Endoscopy-Am. V. Stryker Corp., No. 14-0876-RS (JSC), 2016 WL 7386136, at *8 (N.D. Cal. Dec. 21, 2016)). "'Courts have allowed amendments when the movant made an honest mistake, the request to amend did not appear to be motivated by gamesmanship, or where there was still ample time left in discovery.'" Id. (quoting Karl Storz, 2016 WL 7386136, at *8).

C. DISCUSSION

Google moves to strike Netlist's assertion of claim 16 and the revised priority and conception dates, arguing that these amendments were not authorized by the scheduling order and are not supported by good cause.

1. Good Cause Required

The threshold inquiry is whether Netlist must show good cause to assert claim 16 and the revised priority/conception dates. Netlist argues that, after the case was reopened, amendment of infringement contentions was authorized without express limitation, and thus, good cause need not be shown. This argument is unpersuasive.

The local patent rules, as well as other courts, distinguish between infringement contentions and asserted claims. See PLR 3-1 (providing that a patentee shall serve a "Disclosure of Asserted Claims and Infringement Contentions"); MyGo LLC v. Mission Beach Indus., LLC, No. 16-cv-2350-GPC-RBB, 2018 WL 3438650, at *4 (S.D. Cal. Jul. 17, 2018) (holding that the local patent rules of that district, which allow for "Amended Infringement Contentions" as a matter of right through the filing of a joint claim construction chart, provide

"only for amended infringement contentions, not for amended asserted claims"). Netlist did not specifically seek leave to assert new claims or revised priority/conception dates. Nor was such leave granted. Rather, with Google's agreement, Netlist sought leave to amend only its "infringement contentions," for the stated reason that it was necessary to identify new products now in use. A deadline for "amended infringement contentions" was set on that premise.

Netlist contends MyGo is inapposite because the court in that case found the local rule permitting amendment of "infringement contentions" as a matter of right did not authorize the amendment of asserted claims; the court thus found that a motion demonstrating good cause to amend the asserted claims was required. Netlist argues that the scheduling order in this case "authorized Netlist to ***amend*** its infringement contentions," and thus, a motion to amend was not required. Opp'n at 5 (emphasis in original), Dkt. 170. This misses the point. The only difference between the two cases is that amendment was permitted by local rule in MyGo, whereas amendment was permitted by the scheduling order here. In both cases, however, the allowance of amended "infringement contentions" did not encompass amended asserted claims. Thus, as in MyGo, Netlist was required to file a motion demonstrating good cause.

Netlist's other arguments are likewise unsuccessful. Citing Straight Path IP Grp., Inc. v. Apple Inc., No. C 16-03582 WHA, 2017 WL 3967864, at *5 (N.D. Cal. Sept. 9, 2017), Netlist contends it is "this district's practice" to prohibit a patentee from adding claims in amended infringement contentions "only when the Court explicitly orders as such." Opp'n at 5. The court in Straight Path granted a plaintiff's motion for leave to amend infringement contentions on the express condition that it limit those contentions to the remaining asserted claims. The court did not announce (nor could a sole district judge) or apply a district-wide practice. Although it may have been preferrable if limitations were sought and/or imposed at the time the scheduling order issued in this case, the lack of express limitations is not determinative. In short, absent agreement of the opposing party and authorization of the court, a patentee cannot amend its contentions without a showing of good cause. In obtaining Google's agreement and the district court's authorization, Netlist did not make known its intent to amend the asserted claims or priority/conception dates. Consequently, the scheduling order

did not contemplate or authorize such amendments. A contrary rule would incentivize parties to obfuscate their intent when seeking and obtaining stipulations and orders on such matters.

Finally, Netlist argues that the position advanced by Google is untenable because it would never allow for amendment of asserted claims. Netlist notes that PLR 3-6 speaks only to the amendment of "Infringement Contentions." According to Netlist, an interpretation of the patent rules that distinguishes between "Infringement Contentions" and "Asserted Claims" is untenable in part because it would provide "no express mechanism for a party to amend infringement contentions to assert new claims." Opp'n at 6. This, of course, is incorrect. First, Google does not argue that a patentee may never amend asserted claims, only that doing so requires good cause. Second, as Netlist acknowledges, the local rules must be in accord with the Federal Rules of Civil Procedure. O2 Micro, 467 F.3d at 1366. Although PLR 3-6 fails to mention "Asserted Claims" specifically, it may nonetheless be read to permit a patentee to amend the same, insofar as precluding amendment "might well conflict with the spirit, if not the letter, of the notice pleading and broad discovery regime created by the Federal Rules." Id. However, this is not achieved by contorting the patent rules to eliminate the clear distinction between asserted claims and infringement contentions.

2. Priority and Conception Dates

Netlist argues it acted diligently in asserting revised priority and conception dates because it promptly sought to amend its infringement contentions after the case was reopened. Opp'n at 14. Setting aside the fact that Netlist did not seek or obtain leave to assert revised priority and conception dates, however, this is insufficient to demonstrate diligence. Specifically, Netlist does not address whether it acted diligently in seeking to discover the basis for the amendment or in seeking leave to amend once that basis had been discovered.

The patent local rules require that, not later than 14 days after the initial CMC, a patentee shall disclose the priority date for its asserted claims, PLR 3-1(f), and produce all documents evidencing an earlier conception date, PLR 3-2(b). Courts in this district interpret the local patent rules to require disclosure of a specific conception date, not a date range. Harvatek Corp. v. Cree, Inc., No. C 14-05353 WHA, 2015 WL 4396379, at *2 (N.D. Cal. July

17, 2015); Thought Inc. v. Oracle Corp., No. 12-CV-05601-WHO, 2015 WL 5834064, at *5 (N.D. Cal. Oct. 7, 2015) (reasoning that the purpose of the local patent rules would be frustrated if a patentee could avoid specifying a conception date). These rules "are in place to require patent holders to 'crystallize their theories of the case early in the ligation,' which heads off the possibility of abuse in the form of theories contrived to get behind later-disclosed prior art." Harvatek, 2015 WL 4396379, at *3 (citation omitted). This poses a "minimal burden" for a patent holder, who should have knowledge of the priority and conception dates of its own patented inventions prior to commencing litigation. Id.

Here, in April 2010, Netlist disclosed a priority date of July 1, 2005. It did not disclose an earlier conception date. Google then disclosed its invalidity contentions, the parties conducted discovery, and claim construction briefs were filed. On January 26, 2011, nine months after Netlist served its infringement contentions, the action was stayed. Now, a decade later and after the stay has lifted, Netlist seeks to assert a priority date "as early as March 5, 2004" and a conception date of "no later than mid-2003." The only evidence cited to support these revised dates is the testimony of a named inventor, Jayesh Bhakta, from a deposition taken on September 17, 2010. Had Netlist exercised diligence, it could have worked with Mr. Bhakta to identify the priority/conception dates prior to submitting its April 2010 disclosures or shortly thereafter. At a minimum, however, Netlist should have moved to amend its disclosures after his deposition, which occurred more than three months before the stay. Consequently, Netlist has not acted diligently in asserting its revised priority/conception dates.

Netlist does not address the foregoing, arguing instead that the revised dates are not "new" to Google. Opp'n at 14. That Google was aware of Mr. Bhakta's deposition testimony does not mean it had reason to anticipate Netlist would seek leave to amend its disclosures and rely on these dates, however. Indeed, Netlist did not rely on the newly asserted conception date during the reexamination proceedings, even though various claims of the '912 patent were invalidated based on prior art filed January 5, 2004. Further, as Netlist concedes, "the relevant conception document discussed during deposition … has a date of January 12, 2004." Id. at 15. Although Mr. Bhakta "believed the conception date was in the previous year," no

document evidencing conception in "mid-2003" has been discovered or produced. Id. Thus, even now, Netlist has not identified a specific conception date that predates the relevant prior art. See Harvatek, 2015 WL 4396379, at *1 (striking belated disclosures that the patentee claimed would provide evidence of invention in advance of the filing date, but which failed to identify a specific conception date prior to the previously disclosed priority date).

In view of the foregoing, Netlist has not demonstrated good cause to amend its priority/conception dates. See Harvatek, 2015 WL 4396379, at *1-2 (striking disclosures made two months after the deadline to serve infringement contentions and precluding patentee from asserting a conception date prior to the filing date of the patent application); OpenTV, 2016 WL 3196643, at *1-2 (precluding patentee from asserting conception and reduction to practice dates other than those identified in its infringement disclosures and striking earlier dates proposed for the first time four months after its disclosures were served). Leave to amend the priority/conception dates is therefore denied. See Linex Techs., Inc. v. Hewlett-Packard Co., No. C 13-159 CW, 2013 WL 5955548, at *1 (N.D. Cal. Nov. 6, 2013) (prejudice need not be reached where diligence has not been shown) (citing O2 Micro, 467 F.3d at 1368 (affirming denial of leave to amend upon finding lack of diligence, without reaching issue of prejudice)).[2]

3. Claim 16

a) Diligence

The parties agree that, based on the facts presented, the threshold inquiry is whether Netlist could have asserted claim 16 at the outset of the litigation. Netlist argues it could not. The DDR4 standard was published on September 25, 2012, while this case was stayed. According to Netlist, "only DDR4 DIMMs that comply with certain JEDEC DDR4 standards while operating in PDA [per DRAM addressability] mode (or products that operate in a similar manner) infringe claim 16." Opp'n at 9. Because the DDR2 and DDR3 standards did not

[2] In asserting that amendment would not prejudice Google, Netlist argues that any concern it is attempting to avoid the previously disclosed prior art is misplaced because the PTAB confirmed claim 16 over that prior art and the parties are bound by the PTAB's decision. Opp'n at 15. As Netlist concedes elsewhere in its brief, however, the question of whether the PTAB's decision on claim 16 has preclusive effect on Google is unresolved. Id. at 14 n.11. In any event, as set forth above, leave to amend is denied for lack of diligence.

include the PDA feature, Netlist argues it could not have asserted claim 16 at the outset of the litigation or any time prior to the stay. Netlist further argues, and Google does not dispute, that the period of the stay is excluded from the diligence analysis. See Karl Storz, 2016 WL 2855260, at *6. Regarding the period after February 17, 2021, when the stay was lifted, Netlist notes that it first asserted claim 16 on May 19, 2021, and thereafter served its amended disclosures by the deadline set in the scheduling order, i.e., June 18, 2021. Netlist thus contends it promptly disclosed claim 16 after the case reopened.

Notably, because Netlist did not move for leave to amend its asserted claims before serving its amended disclosures, Google was placed in the position of filing a motion to strike. For this reason, Google's moving papers are somewhat misdirected, as it attempts to show that Netlist was not diligent, without the benefit of Netlist's arguments. See Radware Ltd. v. F5 Networks, Inc., No. 13-02021-RMW, 2014 WL 3728482, at *1 (N.D. Cal. July 28, 2014) ("The burden is on the movant to establish diligence rather than on the opposing party to establish lack of diligence."). Specifically, Google devotes a considerable portion of its motion to arguing that the use of DDR4 technology does not provide good cause for the belated assertion of claim 16 because the '912 patent is not directed to DDR4 technology specifically, but rather, to DDR2 and later technology. As Netlist makes clear in its opposition, however, it does not argue that the '912 patent is directed only to DDR4 technology. Opp'n at 9-10. Rather, Netlist contends that claim 16 *did not* read on DDR2 or DDR3 technology, but *does* read on DDR4 technology, specifically DDR4 DIMMs operating in PDA mode.

Google makes two arguments in response to Netlist's showing of diligence. First, it argues the contention that claim 16 reads on one discrete mode (i.e., PDA) of the DDR4 specification is "meritless." Reply at 4, Dkt. 181. According to Google, claim 16 requires that a "command signal is transmitted to *only one* DDR memory device *at a time*," whereas PDA mode "transmits command signals to *all* of the DDR memory devices in a given rank *at the same time*." Id. (emphasis in original). Google thus argues that "claim 16 is [not] unique to PDA made." Id. Second, it argues that Netlist did not disclose the '912 patent as relevant to

the DDR4 standard when JEDEC promulgated the same.[3] According to Google, this "undercuts any argument that Netlist somehow invented PDA in the '912 [p]atent." Id. at 5.[4]

The thrust of Google's argument is that DDR4 technology operating in PDA mode does not infringe claim 16. Google accurately describes the limitations of claim 16, which discloses a memory module "wherein the command signal is transmitted to only one DDR memory device at a time." Dkt. 170-4 ('912 Patent) at claim 16. Google also presents evidence—slides from a presentation given at the Server Memory Forum 2011, entitled, "DDR4 Module Level Trends and Features"—that describes how PDA mode operates. Dkt. 181-2. The presentation provides a "high level overview" of the technology. Id. at 3. Consistent with Google's assertion, it appears from this evidence that DDR4 DIMMs operating in PDA mode transmit a command signal to all DRAM in a given rank at the same time. Id. at 11-12. This evidence is largely unrebutted by Netlist.[5] Nevertheless, the determination as to whether DDR4 DIMMs operating in PDA mode infringe claim 16 is beyond the scope of the instant motion. See Network Caching Tech., LLC v. Novell, Inc., No. C-01-2079 VRW, 2003 WL 21699799, at *5 (N.D. Cal. Mar. 21, 2003) (explaining that challenges to the merits of a patentee's infringement

[3] JEDEC's Patent Policy requires members to disclose any issued patents or pending applications that are, or may be, relevant to pending or issued standards. The Patent Policy further provides that JEDEC cannot consider a standard that calls for the use of a patented item or process unless the patent holder offers a license.

[4] Netlist objects to evidence offered by Google in support of these arguments, arguing that such evidence may not be offered for the first time in a reply brief. Obj., Dkt. 194. The objection is not well taken. Google's reply evidence directly responds to arguments raised in Netlist's opposition—i.e., that claim 16 reads only on DDR4 technology operating in PDA mode and that no product in use prior to the stay operated in a similar manner. Because Netlist did not move for leave to amend prior to asserting claim 16, Google did not have notice of the basis of Netlist's diligence argument until Netlist filed its opposition brief. In any event, Netlist has responded to the evidence in its objection. Id. at 4-5. The objection is overruled.

[5] At oral argument, Netlist asserted that claim 16 "describes a very precise, almost ballet of how you send signals to the different stack of DRAM." Dkt. 257 at 33:8-10. According to Netlist, "that unique feature is called PDA." Id. Aside from this bare assertion, however, Netlist fails to rebut Google's argument as to what claim 16 discloses. The assertion that claim 16 describes a precise "ballet" also appears to conflict with the language of claim itself, which requires simply that a command signal be sent to one memory device at a time. Netlist further asserts, without additional explanation, that Google's argument is "predicated on an incorrect understanding of how PDA mode works and its narrow construction of the term 'command signal,' disregarding how the term is used in the '912 patent." Obj. at 4.

theories are not meant to be resolved at this stage of the litigation; infringement contentions are not meant to provide "a forum for litigation of the substantive issues").

The focus of our present inquiry is whether DDR4 technology is distinct from prior generations of DDR technology so as to support the belated assertion of claim 16. As to this issue, Google glosses over the innovation of PDA mode. Although DDR4 DIMMs operating in PDA mode may transmit a command signal to all DRAM in a given rank at the same time, Google admits that only selected DRAM "will get programmed by the command signal." Reply at 4; see also Dkt. 181-2 at 11 (explaining that the selected DRAM "will have their mode register programmed differently than the others"). Thus, while older generation technology (e.g., DDR3) programmed all DRAM in a given rank "exactly the same way, [with] no exceptions," PDA mode "solves this problem" and "allows the host to uniquely select individual DRAM to be programmed." Dkt. 181-2 at 7, 8. This is the innovation upon which Netlist relies in asserting claim 16. Accordingly, given that DDR4 technology functions differently than older generation technology, Netlist has shown that it could not have asserted claim 16 prior to the stay.

Google's argument regarding the inadequate disclosure of the '912 patent to JEDEC is likewise ineffectual. Netlist disputes that its disclosures were inadequate, arguing that it disclosed both the '912 patent (and others within the '912 patent family) to the relevant JEDEC committees and subcommittees. See Dkt. 169-13, 169-14. Google responds that those disclosures were specific to DDR2 and DDR3 technology, not DDR4 technology. Reply at 5. Even assuming that Netlist's disclosures were inadequate as it relates to the DDR4 standard, however, it does not follow that the '912 patent is irrelevant to the DDR4 standard generally or PDA mode specifically. Rather, as Google appears to acknowledge in its Counterclaim, see Dkt. 18, the question of whether Netlist properly disclosed the '912 patent to JEDEC is a separate matter. Although an inadequate disclosure may give rise to a counterclaim or even a defense to infringement, it does not preclude the possibility of infringement.

Lastly, Google argues that Netlist was not diligent in the period after the stay lifted because it could have asserted claim 16 sooner. According to Google, Netlist did not require

discovery to accuse DDR4 products of infringing claim 16 because its amended claim chart relies on the public JEDEC standard. Given its reliance on that standard, Netlist likely could have asserted claim 16 at the time the case reopened. Under the circumstances presented, however, Netlist was reasonably diligent in asserting claim 16. Even if Netlist erred in believing that leave to amend infringement contentions also authorized amendment of asserted claims, it reasonably relied on the deadline set forth in the scheduling order to raise all such amendments. See Richtek Tech. Corp. v. uPI Semiconductor Corp., No. C 09-05659 WHA, 2016 WL 3136896, at *2 (N.D. Cal. June 6, 2016) (finding that, even if the alleged infringer could have sought leave to amend much sooner after the stay was lifted, it reasonably relied on a deadline to file invalidity contentions set forth in a scheduling order to pursue the amendments). Netlist served its amended claim chart nearly a month prior to that deadline.

Moreover, the good cause standard does not require "perfect diligence." Facebook, Inc. v. BlackBerry Ltd., No. 18-cv-05434-JSW (JSC), 2020 WL 864934, at *5 (N.D. Cal. Feb. 13, 2020), report and recommendation adopted, 2020 WL 9422395 (N.D. Cal. Mar. 30, 2020). Considering the procedural posture of this case and the nature of the amendment, Netlist was sufficiently diligent in asserting claim 16 approximately three months after the 10-year stay lifted. See Advanced Micro Devices, 2017 WL 732896, at *4 (finding patentee acted diligently in seeking to amend its infringement contentions approximately five months after a 3-year stay lifted where the court had not yet set deadlines for fact or expert discovery and the amendment was made sufficiently in advance of claim construction briefing).

b) Prejudice

Netlist further argues that the assertion of claim 16 will not prejudice Google. As noted by Netlist, "[a]n upcoming discovery deadline tends to loom large in the prejudice analysis." Karl Storz, 2016 WL 2855260, at *7. Here, discovery deadlines have not been set, see Dkt. 117, and the claim construction deadlines initially set after the case reopened have been vacated pending resolution of the parties' motions regarding intervening rights, see Dkt. 192. Courts typically find no prejudice where, as here, the proposed amendments do not pose a risk to discovery and motion deadlines. Karl Storz, 2016 WL 2855260, at *7.

Google does not argue otherwise and identifies no prejudice in terms of its ability to litigate this action. Rather, relying on Capella Photonics, Inc. v. Cisco Systems, Inc., No. 14-cv-03348-EMC, 2019 WL 2359096, at *1 (N.D. Cal. June 4, 2019), Google's argument hinges on the reexamination proceedings. Google asserts that it "relied on Netlist's original identification of asserted claims in deciding which claims to challenge" in the reexamination proceedings. Mot. at 5, Dkt. 153. Specifically, Google did not challenge claim 16. Google notes that it invested time and resources to invalidate the originally asserted claims and succeeded in forcing Netlist to cancel or amend the same. As a result, Google argues, the originally asserted claims are subject to the defense of absolute intervening rights and insulated from infringement liability. According to Google, if Netlist is limited to the originally asserted claims, "there is nothing left to litigate in this case[.]" Id. at 6. On the other hand, if Netlist is permitted to assert claim 16, the reexamination proceedings "will be rendered meaningless," and the action will begin anew as to that claim. Id.

Netlist disputes Google's claim of prejudice, arguing that Google "***did*** raise objections to the validity of claim 16 in the reexamination by and through Inphi and SMT," who Netlist asserts were part of a "Joint Defense Group" with Google. Opp'n at 12 (emphasis in original). This argument is unpersuasive. Although Google, Inphi, and SMT may have had common interests and/or shared counsel at various points in the reexamination proceedings, Netlist cites no evidence or authority to support the argument that these separate entities acted as, or can be treated, as one. That being said, Netlist persuasively argues that the instant action is distinguishable from Capella on several grounds.

In Capella, the civil action was stayed for approximately three years pending *inter partes* review and subsequent appeals. 2019 WL 2369096, at *1. The PTAB found all of the claims originally asserted by the plaintiff to be invalid. The plaintiff appealed the PTAB's decision to the Federal Circuit and the Supreme Court. After the appeals were exhausted, the PTO issued IPR certificates cancelling all of the claims originally asserted in the civil action. Before the PTO issued the IPR certificate, however, the plaintiff filed reissue applications. The plaintiff then moved the district court to extend the stay pending a determination on the reissue

application, or alternatively, for leave to amend its disclosures to assert several new claims. Id. at *1-2. The newly asserted claims were not at issue in the IPR proceedings or the subject of the reissue application but were dependent claims of claims invalidated by the PTAB in the IPR proceedings. Id. at *2. Despite prompting from the district court, the plaintiff failed to provide any explanation as to why it could not have asserted the new claims at the outset of the action. Id. at *3. Reasoning that the plaintiff was "effectively seeking to litigate available claims … twice," the court found that the plaintiff had not been diligent, but instead, was engaged in gamesmanship. Id. at *3-4. Although the court noted that it need not reach the issue of prejudice, it also found that the defendants were "entitled to the certainty and finality which they sought and obtained from the IPR proceedings." Id. at * 6. The court noted that, had the plaintiff asserted the claims initially or sought to add them earlier, the claims may have been adjudicated and possibly invalidated in the IPR proceedings. Id.

Here, unlike in Capella, claim 16 was challenged by Inphi in the reexamination proceedings and determined to be patentable by the PTAB. Thus, while Netlist did not assert claim 16 against Google prior to the issuance of the stay, it cannot be said that Netlist is seeking to "avoid[] the results of the IPR proceedings." Id. at *5; see also Boston Scientific Corp. v. Cook Group Inc., No. 1:17-cv-03448-JRS-MJD, 2021 WL 3634776, at *7 (S.D. Ind. Aug. 16, 2021) (finding defendants were not prejudiced by having to litigate a newly asserted claim that had been challenged in and survived IPR proceedings). Additionally, unlike the patentee in Capella, Netlist has shown that it could not have asserted claim 16 "at the outset" of the litigation. 2019 WL 2359095, at *3. The facts of this case therefore do not support a finding that Netlist is engaged in gamesmanship. Lastly, the originally asserted claims in this case largely were amended, as opposed to canceled, in the reexamination proceedings. Although Google asserts that absolute intervening rights will all but resolve the action as to the originally asserted claims, the reexamination proceedings here did not produce the sort of "certainty and finality" that the IPR proceedings did in Capella. 2019 WL 2359095, at *6. Accordingly, the circumstances in this case militate in favor of granting leave to amend.

III. MOTIONS FOR SUMMARY JUDGMENT

A. RELEVANT BACKGROUND

For purposes of the instant motions, the parties agree that claim 1 of the '912 patent is illustrative. The original claim 1 recited:

> A memory module connectable to a computer system. The memory module comprising:
>
> a printed circuit board;
>
> a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
>
> a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and
>
> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

Dkt. 155-3 ('912 Patent) at claim 1.

As stated above, the '912 patent was subject to reexamination proceedings. During those proceedings, the PTAB invalidated claim 1 (and the other independent claims 15, 28, and 39) based on a combination of prior art references called Amidi and Dell-2. See Dkt. 156-10. In response, Netlist added three additional limitations to distinguish the claims of the '912 patent from the prior art. See Dkt. 155-9. The added limitations are as follows:

> wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,
>
> wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and
>
> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

Dkt. 155-5 ('912 Reexamination Certificate) at claim 1 (italics omitted). The PTAB found the claims patentable as amended. See Dkt. 156-11.

As set forth above, claim 1 requires that the phase-lock loop device be "operatively coupled" to the plurality of DDR memory devices, the logic element, and the register. The specification and prosecution history of the '912 patent does not define or otherwise limit the term "operatively coupled," and thus, it carries its plain and ordinary meaning. During the reexamination proceedings, Netlist urged the examiner to adopt a particular definition of "operatively coupled" in an attempt to distinguish the '912 patent from prior art. Dkt. 155-10 at 41-12. Specifically, Netlist argued that "operatively coupled" means "the operations of the logic element 40 are clocked either directly or indirectly (e.g., through a clock buffer) by the output of the PPL 50," i.e., "the output of the PLL 50 controls the operation of the logic element 40." Id. at 40.

The original claim 16 depended on claim 15. It recited: "The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time." Dkt. 155-3 ('912 Patent) at claim 16. On April 4, 2011, the examiner rejected claim 15 but confirmed the patentability of claim 16. See Dkt. 156-5. In a subsequent office action dated October 14, 2011, the examiner reiterated that claim 16 was "unamended" and confirmed. See

Dkt. 156-7. In the response that followed, Netlist rewrote original claim 16 in independent form, incorporating verbatim the limitations of original claim 15. Dkt. 156-8 at 9-10. In an office action dated November 13, 2012, the examiner recognized that claim 16 and several others had been "rewritten in independent form maintaining their original scope." Dkt. 156-9 at 6. As stated above, Netlist eventually amended claim 15 to include new limitations, and the PTAB determined that claim 15 was patentable as amended. The new limitations added to amended claim 15 were not included in claim 16, however; only the language of original claim 15 was incorporated. See Dkt. 155-5 ('912 Reexamination Certificate) at claim 16.

On February 8, 2021, the PTO issued the reexamination certificate, which provides:

> Claims 2, 5, 7, 9, 21, 23, 25, 26, 30, 33, 42, 44, and 51 are cancelled.
>
> Claims 1, 15, 16, 28, 39 and 43 are determined to be patentable as amended.
>
> Claims 3, 4, 6, 8, 10-14, 17-20, 22, 24, 27, 29, 31, 32, 34-38, 40, 41 and 45-50, dependent on an amended claim, are determined to be patentable.
>
> New claims 52-91 are added and determined to be patentable.

Dkt. 155-5 ('912 Reexamination Certificate) at 2. After the reexamination certificate issued and the stay of this action lifted, Netlist served amended infringement contentions, asserting 64 claims (including claim 16) against 5 categories of accused products, i.e., 4-Rank DDR2 FBDIMMs, 4-Rank DDR3 LRDIMMs, 4-Rank DDR4 NVDIMMs, 4-Rank DDR4 RDIMMs, and 4-Rank DDR4 LRDIMMs. Dkt. 154-8. The parties thereafter acknowledged that the reexamination proceedings may give rise to a defense of absolute intervening rights and sought early resolution of the issue.

B. LEGAL STANDARDS

1. Summary Judgement

A party may move for summary judgment on some or all of the claims or defenses presented in an action. Fed. R. Civ. P. 56(a)(1). "Summary judgment is appropriate only where 'there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law.'" Salazar-Limon v. City of Houston, 137 S. Ct. 1277, 1280 (2017) (quoting Fed. R. Civ. P. 56(a)). The moving party bears the initial burden of identifying those portions of the pleadings, discovery, and affidavits that establish the absence of a genuine

dispute of material fact. Cline v. Indus. Maint. Eng'g & Contracting Co., 200 F.3d 1223, 1229 (9th Cir. 2000) (citing Celotex Corp. v. Catrett, 477 U.S. 317, 323-25 (1986)). If the moving party meets its burden, the burden then shifts to the non-moving party to go beyond the pleadings and identify specific facts demonstrating the existence of a genuine issue of material fact. Id. (citing Celotex, 477 U.S. at 323-24). On a motion for summary judgment, all reasonable inferences are to be drawn in favor of the party against whom summary judgment is sought. Matsushita Elec. Indus. Co. v. Zenith Radio Corp., 475 U.S. 574, 587 (1986).

2. Intervening Rights

"The doctrine of intervening rights first developed as courts recognized that permitting substantive changes to the scope of patent claims through post-issuance procedures left 'the door …open for gross injustice' where a third party, having already begun to make, use or sell a given article, finds its previously lawful activities rendered newly infringing under a modified patent." Marine Polymer Techs., Inc. v. HemCom, Inc., 672 F.3d 1350, 1361 (Fed. Cir. 2012) (*en banc*) (quoting Sontag Chain Stores Co. v. Nat'l Nut Co., 310 U.S. 281, 293-95 (1940)).

With respect to reissued patents, the intervening rights doctrine was codified by the Patent Act of 1952. 35 U.S.C. § 252. Section 252 provides for two types of intervening rights: absolute and equitable. As is pertinent here, absolute intervening rights "abrogate liability for infringing claims added to or modified from the original patent if the accused products were made or used before the reissue[.]" Marine Polymer, 672 F.3d at 1361-62. "Intervening rights do not accrue, however, where the accused product or activity infringes a claim that existed in the original patent and remains 'without substantive change' after reissue." Id. at 1362 (quoting Seattle Box Co. v. Indus. Crating & Packing, Inc., 731 F.2d 818, 827-28 (Fed. Cir. 1984)). Although the doctrine of intervening rights originated in the context of reissue proceedings, it has since been extended to reexamination proceedings. Id.; see 35 U.S.C. §§ 307(b) (governing *ex parte* reexamine), 316(b) (governing *inter partes* reexamination).[6]

[6] Citations to section 316(b) refer to the former version of the statute (effective Nov. 2, 2002 to Sept. 15, 2012) in existence prior to the America Invents Act ("AIA"), which replaced *inter partes* reexamination with *inter partes* review.

In deciding "whether intervening rights arose from a reexamination," the first inquiry is "whether the asserted claim is 'amended or new[.]'" Marine Polymer, 672 F.3d at 1363. "Only if the claim at issue is new or has been amended may the court proceed to the second step in the analysis and assess the substantive effect of any such change pursuant to § 252." Id. The second inquiry is whether the original and reexamined claims are "substantially identical." 35 U.S.C. §§ 252. "Reexamined claims are 'identical' to their original counterparts if they are 'without substantive change.'" Laitram Corp. v. NEC Corp., 163 F.3d 1342, 1346 (Fed. Cir. 1998) (quoting Seattle Box, 731 F.2d at 827-28)). "[I]n determining whether substantive changes have been made, [the court] must discern whether the *scope* of the claims are identical, not merely whether different words are used." Id. (emphasis in original).

C. DISCUSSION

Google moves for summary judgment on the issue of absolute intervening rights, seeking an order that the accused products it purchased and/or used prior to February 8, 2021 are subject to this defense. Netlist opposes Google's motion and separately moves for partial summary judgment, seeking an order that Google is not entitled to a defense of intervening rights with respect to claim 16. Because the issues with respect to claim 16 are distinct, it is analyzed separately below. The remaining claims fall into two categories: claims determined to be patentable as amended (the "Amended Claims") and claims added during re-examination (the "Added Claims"). The Amended and Added Claims are addressed together.

1. The Amended and Added Claims

The first inquiry in the intervening rights analysis is whether a claim is "amended or new." With the exception of claim 16 (discussed below), Netlist does not dispute that the asserted claims are amended or new. The pertinent inquiry, then, is whether the scope of the claims have been substantively changed. Google argues that Netlist "substantively narrowed the scope of the [Amended Claims]" in the reexamination proceedings "through detailed amendments and arguments designed to avoid the prior art." Def.'s Mot. at 7-8, Dkt. 155. Google further argues that Netlist drafted the Added Claims "to have the same narrow scope as the [A]mended [C]laims." Id. at 8. Google then identifies four specific ways in

which it contends Netlist substantively changed the scope of the claims, i.e., by adding the limitations identified above with respect to (1) the "phase-lock loop device," (2) the "register," and (3) the "logic element," and by proposing a new definition of (4) "operatively coupled."

a) Suitability for Resolution

The Federal Circuit has held that "a claim amendment made during reexamination following a prior art rejection is not *per se* a substantive change." Laitram, 163 F.3d at 1347 (citation omitted). "Rather, to determine whether a claim change is substantive it is necessary to analyze the claims of the original and the reexamined patents in light of the particular facts, including the prior art, the prosecution history, other claims, and any other pertinent information." Id. (quotation marks, citation, and alteration omitted). "In determining the scope of the claims, [courts] apply the traditional claim construction principles of Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*), paying particular attention to the examiner's focus in allowing the claims after amendment." Convolve, Inc. v. Compaq Computer Corp., 812 F.3d 1313, 1322-23 (Fed. Cir. 2016) (quotation marks and citations omitted); see also Laitram, 163 F.3d at 1348 (holding that, where amendments result in the allowance of claims that had been rejected over prior art, that "is a highly influential piece of prosecution history").

Although the examiner's allowance of amended claims is significant, courts must account for differences between the broadest reasonable interpretation ("BRI") standard, applied by examiners during reexamination proceedings, and the Phillips standard, applied by courts in infringement proceedings. Convolve, 812 F.3d at 1325. Under the Phillips standard, claim terms are given the meaning that would be ascribed to them by a person of ordinary skill in the art ("POSITA"), whereas, under the BRI standard, claim terms are given the broadest reasonable interpretation consistent with the specification. In re CSB-Sys. Int'l, Inc., 832 F.3d 1335, 1340 (Fed. Cir. 2016) (add citations). Although "[i]n many cases, the claim construction will be the same under both standards," this is not always the case. Id. at 1341. Thus, an examiner's finding that a claim did not include a certain limitation, standing alone, "cannot be dispositive." Convolve, 812 F.3d at 1325; see also Laitram, 163 F.3d at 1348 ("Although it is difficult to conceive of many situations in which the scope of a rejected claim that became

allowable when amended is not substantively changed by the amendment, we arrive at our conclusion, not through any 'per se rule,' but in light of an overall examination of the written description, the prosecution history and the language of the respective claims.").

Invoking the forgoing standards, Netlist makes two threshold arguments that Google's motion for summary judgment fails as a matter of law: (1) Google improperly relies on a *per se* rule that claims amended during reexamination to avoid prior art are substantively changed; and (2) Google fails to present the requisite claim construction analysis for the original claims, Pl.'s Opp'n at 14-16, 13-14, Dkt. 197. These arguments are unpersuasive. The assertion that Google "reduces the test for absolute intervening rights to the very *per se* rule the Federal Circuit has rejected multiple times[,]" id. at 15, is simply untrue. Although Google emphasizes that the claims were amended to avoid prior art—a fact described by the Federal Circuit as "a highly influential piece of prosecution history"—it does not rely on this fact alone. Rather, Google discusses the language of the original and amended claims, the prosecution history of the '912 patent, and the relevant prior art. See Def.'s Mot. at 7-15.

The assertion that further claim construction is required also misses the mark. In support of this argument, Netlist cites a handful of district court cases that declined to resolve the issue of claim identicality before claim construction had occurred. See, e.g., Etagz, Inc. v. Quicksilver, Inc., No. 10-300, 2012 WL 2135497, at *2 (C.D. Cal. June 11, 2012). The cases reason that courts must analyze the scope of claims when ruling on identicality, and thus, the determination is more appropriately resolved during claim construction proceedings. Id. As acknowledged by Netlist, see Pl.'s Opp'n at 14 n.4, however, a claim construction hearing was conducted twelve years ago in the related case, Google v. Netlist, No. 08-cv-4011, Dkt. 79 (N.D. Cal. Nov. 16, 2009), with respect to U.S. Patent No. 7,289,386 ("the '386 patent"), of which the '912 patent is a continuation. Prior to the stay in this action, the parties submitted agreed-upon constructions for various claim terms of the '912 patent, including the terms previously construed in the related case. Dkt. 45. As is pertinent here, the parties agreed to constructions for the claim terms "logic element," "register," and "phase-lock loop device." Id., Ex. A. Netlist does not repudiate those constructions, and in fact, argued at the hearing on

the instant motions that those constructions support its argument regarding claim scope. See Dkt. 257 at 19-20. Given that the parties' agreed-upon constructions are already in the record, it is unnecessary for Google to present anything further in that respect.[7]

b) The Added Limitations

Turning to the merits of the second inquiry of the intervening rights analysis, the scope of the claims narrowed during the reexamination proceedings. "[A] plain reading of the claims … indicate[s] that the original and reexamined claims are of a different scope[.]" Laitram, 163 F.3d at 1348. Netlist added nearly 200 words to the claims in three separate limitations. Although the focus of the inquiry is the substance of the claims, not the mere number of words added, the breadth of the amendments bears noting. Indeed, this is not a case in which a patentee added a one- or two-word "modifier" to existing claim terms. Cf. Convolve, 812 F.3d at 1323 (holding that addition of the word "seek" in front of "acoustic noise" did not alter the scope of the claims where the specification and prosecution history demonstrated that the original claims were limited to seek acoustic noise). Rather, extensive amendments were made. Nor is this a case in which descriptive language was added "simply to further clarify the completely sufficient language used in the original claims." Kaufman Co. v. Lantech, Inc., 807 F.2d 970, 977 (Fed. Civ. 1986) (holding that addition of approximately 25 words did not alter the scope of the claims where the language "was already present in the specification and in the original claims themselves … almost to the point … that some of the amendments made were unnecessary and redundant"). Though some of the added language was present in the specification, much was new, and none appeared in the original claims themselves. The primary authorities relied upon by Netlist—Convolve and Kaufman—are thus readily distinguishable. With that in mind, we turn to the substance of the amendments, with particular focus on the added limitations that were crucial to the allowance of the claims.

[7] Netlist briefly raises a discovery issue, arguing that Google was ordered fully to answer an interrogatory regarding the basis for its intervening rights defense but failed to provide any detailed claim construction argument in its response. Pl.'s Opp'n at 14. It is not apparent that a detailed claim construction argument was required in response to the interrogatory at issue. Even if it were, however, Netlist has not brought any motion to enforce the discovery order or to impose sanctions.

The parties agree that "phase-lock loop device" means "a device for generating a clock signal that is related to the phase of an input reference signal." Dkt. 45, Ex. A. The original claim 1 required a phase-lock loop device that was a) mounted to the printed circuit board and b) operatively coupled to the plurality of DDR memory devices, the logic element, and the register. Original claim 1 was rejected as obvious over Amidi. In pertinent part, the examiner determined that Amidi discloses a phase-lock loop device operatively coupled to a plurality of memory devices, a logic element, and a register. See Dkt. 197-4 at 19-20. Netlist amended claim 1 to require that the phase-lock loop device transmit a PLL clock signal to each of the coupled components. See Dkt. 155-9 at 48. When submitting the proposed amendments, Netlist argued that, although Amidi transmits a PLL clock signal to the memory devices and the register, it does not transmit a PLL clock signal to the logic element. Id. at 51. Because Amidi did not disclose transmission of a PLL clock signal to the logic element, it also failed to disclose a logic element generating output signals in response to a PLL clock signal (as amended claim 1 now does). Id. at 52.

The parties further agree that "logic element" means "a hardware circuit that performs a predefined function on input signals from the computer system and presents the resulting signals as its output." Dkt. 45, Ex. A. As stated above, original claim 1 required that the logic element receive a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal. It also required that the circuit generate a set of output control signals in response to the set of input control signals. Original claim 1 was rejected as obvious over Amidi in view of Dell-2. Netlist amended claim 1 to require that a) the "at least one row/column address signal" received by the logic element be comprised of "at least one row address signal" and b) this row address signal be separate from the plurality of row/column address signals received by the register. See Dkt. 155-9 at 49. Amended claim 1 also now requires that the logic element generate gated column access strobe (CAS) or chip-select signals in response at least in part to i) the at least one row address signal; ii) the bank address signals; 3) the at least one chip-select signal of the set of input control signals; and iv) the PLL

clock signal. Id. When submitting the proposed amendments, Netlist argued that Amidi does not use bank address signals (or the combination of bank address signals and at least one row address signal) to general control signals. Id. at 52-53.

Based on the foregoing, the "phase-lock loop device" and "logic element" limitations narrowed the scope of the claims.[8] Whereas the memory module of original claim 1 did not require either a PLL clock signal transmitted to the logic element or the use of a combination of bank address signals and at least one row address signal to generate control signals, the memory module of amended claim 1 requires both. See Laitram, 163 F.3d at 1348 (holding the scope of original and reexamined claims differed where the original claims covered a printer or method of printing that "generated *any* quality of alphanumeric characters," while the amended claims covered only a printer or method of printing that generated "'*type quality*' alphanumeric characters") (emphasis in original). As demonstrated, these added limitations were crucial to the allowance of the claim because they overcome rejections based on Amidi and Dell-2. See id. (holding scope of the claims was substantively changed where, "the addition of the 'type quality' limitation, along with the other amendments, resulted in the allowance of the claims that had been rejected in the reexamination proceeding over prior art"). As recognized by the Federal Circuit, this is a "highly influential piece of prosecution history." Id.[9]

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[8] Google also relies on the added "register" limitation. It appears the requirement that the logic element receive a row address signal separate from the plurality of row/column address signals received by the register may have been crucial to the allowance of the amended claim. However, without deciding the issue, it is not apparent that the register limitation, standing alone, was crucial. Because a finding that any one of the added limitations substantively changed the scope of the claim is dispositive, the register limitation is not separately addressed. See Laitram, 163 F.3d at 1345 (concluding that one of three added limitations changed the scope of the claims and declining to reach the other two).

[9] In concluding that amendments were clarifying, as opposed to narrowing, the Federal Circuit in Convolve declined to give "significant weight" to the patentee's and examiner's use of the term "clarify" or "clarifying" to describe the amendments. 812 F.3d at 1325. Although such statements are not given significant weight here, it is noted that, during the reexamination proceedings and subsequent appeal, Netlist repeatedly described the amendments as performing a narrowing function. For example, in its appeal brief, Netlist stated that it had "narrowed its claims" to require a memory module with a logic element that acts in response at least in part to four enumerated signals" and "unequivocally disclaimed any broader meaning." Dkt. 208-3 at 1-2. Netlist also argued before the PTAB that it had "narrowed" the claims to overcome the rejection based on prior art. Dkt. 155-9 at 47, 51.

In arguing to the contrary, Netlist relies on the declaration of its litigation expert, Murali Annavaram ("Dr. Annavaram"), to suggest that a POSITA would understand that the added limitations were inherent in the original claims. In other words, Netlist contends the amendments were merely clarifying. As discussed below, the evidence does not support this contention. Regarding the phase-lock loop limitation, Dr. Annavaram opines that a phase-lock loop device ("PLL"), by definition, performs the specific function of generating a clock signal. Dkt. 197-9 ¶ 23. According to Dr. Annavaram, "[t]he registers and logic elements in a design such as the claimed circuit in the '912 patent need clocks to operate." Id. He further opines that "[t]he only function performed by the disclosed PLL device in the '912 patent is providing a clock signal; the written description makes no mention of any other source of clock signals other than the PLL." Id. Regarding the logic element limitation, Dr. Annavaram opines that, based on his opinion regarding the PLL, and as illustrated in Figure 1A of the '912 patent, a POISTA would understand that the logic element required clock signals from the PLL to function. Id. ¶ 31. Relying again on Figure 1A, Dr. Annavaram further opines that original claim 1 disclosed a logic element that received at least one row address bit, the chip-select signals, and bank address signals. Id. ¶ 34.

As a threshold matter, Dr. Annavaram's declaration is afforded little weight. At his deposition, Dr. Annavaram appeared unwilling or unable to answer basic questions, largely limiting his testimony to whether or not his declaration offered an opinion on such matters. See, e.g., Dkt. 208-4 at 95:9-97-3, 63:17-68:14. As noted by Google, Dr. Annavaram also testified that his declaration had not provided a claim construction analysis and that he had not applied claim construction standards. Id. at 49:7-21. Moreover, during his deposition, Dr. Annavaram contradicted and/or undermined the opinions offered in his declaration. As is pertinent here, Dr. Annavaram admitted that he erred in asserting the original claims required a logic element that receives a "row address signal." Rather, Figure 1A shows the logic element receiving a "row/column address signal," which the patent clearly shows to be broader. Id. at 60:9-61:8, 70:6-72:15, 90:1-6. Dr. Annavaram also did not dispute that, although certain embodiments of the '912 patent describe a phase-lock loop device transmitting a clock signal

to the logic element, the patent's specification does not exclude other embodiments that use an external clock signal (as Amidi does). Id. at 86:8-87:8. This undermines the previous suggestion that the PLL of original claim 1 had to provide a clock signal to the logic element.

More fundamentally, however, Dr. Annavaram's opinions simply do not address all aspects of the added limitations and are unsupported by the specification of the '912 patent. Setting aside the error in Dr. Annavaram's opinion that the logic element of original claim 1 receives specific signals, the added logic element limitation requires, not only that the logic element *receive* those signals, but that it *generate* CAS or chip-select signals *in response to* these signals (as well as the PLL clock signal). Dr. Annavaram's declaration is silent on this matter. The relevant portions of Dr. Annavaram's opinions are also based on Figure 1A of the '912 patent. As Dr. Annavaram acknowledged at his deposition, however, Figure 1A is merely a preferred embodiment of the invention. See id. at 73:3-12; 861-16. It is well-settled that embodiments appearing in a specification will not be read into the claims where the claim language is boarder than the embodiments. Laitram, 163 F.3d at 1348 (rejecting the patentee's "invitation … to read a limitation into the original claims that is simply not there"); see also GE Lighting Sols., LLC v. AgiLight, Inc., 750 F.3d 1304, 1309 (Fed. Cir. 2014) (holding the district court erred by reading limitations from a preferred embodiment into the claims). In view of the foregoing, it is clear that the added phase-lock loop and logic element limitations narrowed the scope of the '912 patent.

c) Prosecution Disclaimer

In addition to relying on the added limitations discussed above, Google argues that Netlist narrowed the Amended and Added Claims through prosecution disclaimer by proposing a narrower definition of "operatively coupled" during the reexamination. The issue of whether prosecution disclaimer may give rise to intervening rights is addressed as to claim 16 in Section II.C.2.b.ii., *infra*. Here, given that the added limitations described above substantively changed the scope of the Amended and Added Claims, the issue of prosecution disclaimer need not be reached. See Laitram, 163 F.3d at 1345 (concluding that one of three added limitations

changed the scope of the claims and declining to reach the other two). In view of the foregoing, the Amended and Added Claims are subject to absolute intervening rights.

2. Claim 16

As set forth above, during the reexamination proceedings, claim 16 was rewritten in independent form; no other changes were made. In light of the foregoing, Netlist argues that claim 16 is not "amended or new," and even if it were, the claim scope is identical. Google argues that claim 16 is technically amended and that its claim scope was narrowed through: (1) prosecution disclaimer; and (2) surrender of equivalents.

a) Amended or New

As stated above, the first question in the intervening rights analysis is whether the claim is "amended or new." Google acknowledges that claim 16 was merely rewritten in independent form, but nonetheless relies on the fact that the claim was "literally amended." Def.'s Opp'n at 8, Dkt. 195. As support, Google emphasizes that the reexamination certificate identifies claim 16 as "amended." Id. at 7. Netlist responds that Google's argument elevates form over substance, in disregard of both the reexamination history of claim 16 and Federal Circuit authority regarding the application of § 316. Netlist's argument is the more persuasive.

The Federal Circuit has explained that § 316 "identifies three categories of claims in a reexamined patent: (1) claims that existed in the original patent but have been cancelled as unpatentable, (2) claims that existed in the original patent and have been confirmed as patentable, and (3) amended or new claims that did not exist in the original patent but have been found to be patentable and will be incorporated into the patent by the PTO." Marine Polymer, 672 F.3d at 1363-64. "In providing for intervening rights, [§ 316(b)] is limited to the third category of claims…." Id. at 1364.[10] Here, claim 16 was confirmed on

[10] Marine Polymer concerned *ex parte* reexamination proceedings under § 307(b). As noted by the Federal Circuit, however, the language of pre-AIA §§ 307(b) and 316(b) are "essentially identical." Marine Polymer, 672 F.3d at 1362 & n.8.

reexamination to be patentable *as originally issued*. It thus falls within the second category of claims described in Marine Polymer, to which intervening rights do not apply.

Claim 16 was thereafter rewritten in independent form in accordance with MPEP § 2660.03 (providing that, when an amended base claim is rejected, a claim dependent thereon must be rewritten in independent form). As noted by Netlist, however, "[a] claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers." 35 U.S.C. § 112(d); see also Bloom Eng'g Co. v. N. Am. Mfg. Co., 129 F.3d 1247, 1250 (Fed. Cir. 1997). Claim 16 therefore remains unchanged and has not been "amended," as that term is used in the context of patent prosecution. Marine Polymer, 672 F.3d at 1364 ("'[A]mended' is a term of art in patent prosecution, including reexamination proceedings, and in that context connotes formal changes to the actual language of a claim."). A claim cannot be "amended" for purposes of § 316(b) "without changing the claim language itself." Id.; see also id. at 1363 (explaining that the patent claims asserted against the alleged infringer were not new or amended where they contained "identical language before *and* after reexamination") (emphasis in original).[11]

To be sure, claim 16 is technically labeled "amended" in the reexamination certificate. Yet, as discussed above, this conflicts with the history of the reexamination proceedings. Indeed, the reexamination certificate identifies claim 16, not only as "amended," but "determined to be patentable as amended." This is incorrect, as claim 16 was determined to be patentable *as originally issued*. "[T]he plain directive" of § 316(b)

[11] In a footnote, Google argues that claim 16 falls within a definition of "amended" set forth in Marine Polymer. Def.'s Opp'n at 8 n.5 (citing Marine Polymer, 672 F.3d at 1363 ("In general parlance, 'amend' means 'to alter … formally by adding, deleting, or rephrasing.") (quoting Am. Heritage College Dict., 42-43 (3d ed. 1997)). According to Google, claim 16 was amended because the limitations of claim 15 were "added." Id. As an initial matter, after setting forth the generic definition of "amend" cited by Google, the Federal Circuit held that "amended" is a term of art and provided a specific definition of the term in the context of patent prosecution. Id. at 1364. Moreover, even applying the definition cited by Google, claim 16 is not amended because, as described above, the limitations of claim 15 were incorporated into the claim by reference. If Google's argument were adopted, patentees would likely stop writing claims in dependent form, with the only tangible result being lengthier patents.

does not permit the invocation of intervening rights "against claims that the PTO confirmed on reexamination to be patentable as originally issued." Marine Polymer, 672 F.3d at 1365.

Finally, Google asserts that nothing in § 316(b) "excludes amendments that are made to rewrite a claim from dependent to independent form." Def.'s Opp'n at 8. Google argues it is impermissible to read such a restriction into the statute. Application of this maxim of statutory construction is inapplicable here. For one thing, Marine Polymer interprets the term "amended" in the context of § 316(b); it does not add restrictions to the statute. For another, Google's argument divorces the term "amended" from the broader context—and purpose—of the statute. See Marine Polymer, 672 F.3d at 1361 (the purpose of the intervening rights doctrine is to prevent injustice where previously lawful activities are rendered "newly infringing" under a modified patent); see also P.J. Frederico, Commentary on the New Patent Act, 75 J. Pat. & Trademark Off. Soc'y 161, 206-207 (1993) (reprinted from 35 U.S.C.A. 1954 ed.) ("The statute gives a simple test for determining when intervening rights cannot be present and this is whether claims of the original patent which are repeated in the reissue are infringed. If the reissued patent has valid claims in it which were also in the original patent, and these claims are infringed, then the question of intervening rights cannot arise.").

b) Scope

Even if claim 16 were technically amended so as to satisfy the first step of the intervening rights inquiry, the defense fails at the second step. Rewriting a dependent claim in independent form does not constitute a substantive change in claim scope. Bloom, 129 F.3d at 1250 (holding that restating a dependent claim in independent form does not change the scope of the claim); see also Sonos, Inc. v. D&M Holdings Inc., No. CV 14-1330-WCB, 2017 WL 4969330, at *5 (D. Del. Nov. 1, 2017) (finding that writing dependent claims in independent form "was a cosmetic change, not a substantive one" and "does not give rise to intervening rights"); Dexcowin Glob., Inc. v. Aribex, Inc., No. CV 16-143-GW(AGRX), 2017 WL 3477748, at *14 (C.D. Cal. June 7, 2017) (finding there could be "no dispute" that certain claims "would not trigger intervening rights, because they were

merely amended from dependent to independent form"); SignalQuest, Inc. v. Chou, No. 11-CV-392-JL, 2016 WL 738209, at *4 (D.N.H. Feb. 23, 2016) (finding no intervening rights where claims rewritten in independent form were "identical in scope to original dependent claims"). The rationale for this is clear—rewriting a dependent claim in independent form merely makes "explicit" what was previously incorporated by reference. Safoco, Inc. v. Cameron Int'l Corp., No. 4:05-CV-00739, 2009 WL 10742813, at *9 (S.D. Tex. Apr. 9, 2009), report and rec. adopted, 2009 WL 10695587 (S.D. Tex. May 8, 2009) (citing 35 U.S.C. § 112; Bloom, 129 F.3d at 1250). Google does not argue otherwise, but nonetheless claims that claim 16 was narrowed through: (1) prosecution disclaimer; and (2) surrender of equivalents. These arguments are unsupported and, ultimately, unsuccessful.

i. Prosecution Disclaimer

Arguments made before the PTO may give rise to prosecution disclaimer. Tech. Properties Ltd. LLC v. Huawei Techs. Co., 849 F.3d 1349, 1357 (Fed. Cir. 2017). Google contends that Netlist narrowed the scope of claim 16 through prosecution disclaimer by arguing in favor of a narrower definition of the term "operatively coupled" during the reexamination proceedings. Relying on Marine Polymer, Netlist responds that prosecution disclaimer cannot give rise to intervening rights as a matter of law.

As discussed above, the Federal Circuit in Marine Polymer considered whether argument alone can give rise to intervening rights. It held that a claim is not "amended," and thus, not subject to intervening rights, without "formal changes to the actual language of a claim." 672 F.3d at 1364. Google emphasizes that the Federal Circuit made this determination in the context of the first step of the intervening rights inquiry. See Def.'s Opp'n at 13. Google fails, however, to explain effectively why the teachings of Marine Polymer cannot (and should not) inform our analysis at the second step of the inquiry.

In Marine Polymer, the accused infringer argued that reexamination proceedings gave rise to intervening rights because the patentee had narrowed the scope of its claims by persuading the examiner to adopt a particular construction of "biocompatible." 672 F.3d at 1360-61. In rejecting that argument, the Federal Circuit stated:

> HemCon sidesteps [the issue of whether a claim is amended or new] by emphasizing the well-recognized principle that arguments made during prosecution can affect the ultimate meaning of a claim term—and thus the "scope" of a claim—and then returning to its contention that intervening rights turn on whether claim scope changes during reexamination. HemCon thus posits that Marine Polymer's actions in reexamination rendered the asserted claims effectively 'amended' by disavowal or estoppel, even though the language of the claims was not formally changed. We disagree.

Id. at 1363. Thus, despite recognizing that arguments made during reexamination proceedings "can affect the proper interpretation and effective scope of" a claim, the Federal Circuit held that such argument, standing alone, cannot give rise to intervening rights. Id. at 1365. A finding that argument can give rise to intervening rights where claim language is technically changed, even if that change does not itself alter the scope of a claim (e.g., where a dependent claim is rewritten in independent form) would be incongruous with that holding. Such a finding would give rise to different results based on nothing more than a mere technicality.[12]

Google offers no authority to the contrary. Google cites Huawei, 849 F.3d at 1357, which holds that argument made before the PTO may give rise to prosecution disclaimer. This tenet of patent law is undisputed and was recognized in Marine Polymer. 672 F.3d at 1363 ("claims are properly interpreted to account for arguments and concessions made during prosecution"). Huawei did not involve intervening rights, however, and says nothing about whether prosecution disclaimer constitutes a substantive change in claim scope giving rise to intervening rights.

[12] In Marine Polymer, the Federal Circuit dismissed the accused infringer's concern of gamesmanship, i.e., that "shrewd patentees" would simply rely on arguments rather than amendments during reexamination, thereby avoiding intervening rights. 672 F.3d at 1364. The Federal Circuit reasoned that, if an examiner determines that a claim must be amended to be allowable, the examiner would be expected to require amendment rather than accept argument alone. Id. Indeed, the Federal Circuit stated that Congress may have expected changes in claim scope during reexamination to be made by amendment, which "would avoid the risk of creating a loophole in the intervening rights defense." Id. Moreover, the Federal Circuit posited that, if argument alone is sufficient to overcome a rejection, it is probably because the claims at issue are allowable. Id. This reasoning supports a finding that, where technical amendments do not alter the scope of a claim, argument alone cannot.

The sole case cited by Google for that proposition is Dey, Inc. v. Sepracor Inc., 847 F. Supp. 2d 541, 559 (S.D.N.Y. 2012), rev'd and remanded sub nom. Dey, L.P. v. Sunovion Pharms, Inc., 715 F.3d 1351 (Fed. Cir. 2013), which, in turn, cites Univ. of Va. Pat. Found. v. Gen. Elec. Co. ("Pat. Found."), 755 F. Supp. 2d 738, 747-48 (W.D. Va. 2011). Although not essential to its findings, Dey stated that "[a] prosecution disclaimer can operate as a 'substantive change' that limits damages under § 252 and § 307." Id. This dictum—for which Dey offers no independent analysis or support—is neither binding nor persuasive. Pat. Found. was decided prior to, and considered the same ultimate question as, Marine Polymer. 755 F. Supp. 2d at 747-48 (considering, as a matter of first impression, "[w]hether the term 'amended' limits the application of § 307(b) to only explicit wording changes, as opposed to changes through other means—such as prosecution disclaimer"). Given that the Federal Circuit *en banc* in Marine Polymer reached the opposite conclusion as the district court in Pat. Found., the latter case is no longer good law.

In sum, Google points to no case in which prosecution disclaimer alone gave rise to intervening rights, and such notion is contrary to the teachings of Marine Polymer, even where the first step of the intervening rights analysis has been satisfied. As the Federal Circuit stated in Bloom, intervening rights do not apply where "a claim granted or confirmed upon reexamination is identical to an original claim." 129 F.3d at 1250. For the reasons set forth above, claim 16 is identical to an original claim. Accordingly, prosecution history alone will not support a defense of intervening rights. In view of this finding, the parties' remaining arguments—as to whether prosecution disclaimer should be found on the facts here—need not be reached.

ii. Surrender of Equivalents

The doctrine of equivalents allows a patent holder to assert infringement against a product or process that is not within the literal scope of the claims "if there is 'equivalence' between the element of the accused product or process and the claimed elements of the patented invention." Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co., 520 U.S. 17, 21 (1997). Prosecution history estoppel may bar a patentee from asserting equivalents,

however, "when an amendment is made to secure the patent and the amendment narrows the patent's scope." Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd., 535 U.S. 722, 736 (2002). Such amendments give rise to a presumptive surrender of equivalents. Id.

In Honeywell Int'l Inc. v. Hamilton Sundstrand Corp., 370 F.3d 1131, 1141 (Fed. Cir. 2004), the Federal Circuit held that rewriting a dependent claim in independent form, coupled with cancellation of the original independent claim to which it referred, gives rise to a presumptive surrender of equivalents. Relying on Honeywell, Google suggests that the surrender of equivalents, in turn, narrows the scope of claim 16, thereby giving rise to intervening rights. Google's argument is unsupported. Tellingly, although Honeywell was decided in 2004, Google cites no case predicating a finding of intervening rights on the surrender of equivalents. This is unsurprising, given that Honeywell did not involve intervening rights, 370 F.3d at 1136 ("Only infringement under the doctrine of equivalents is at issue in this appeal"), and cannot be read to endorse an extension of the defense based on the surrender of equivalents. See Safoco, 2009 WL 10742813, at *10 (finding attempt to introduce surrender of equivalents into an intervening rights analysis unsupported by Honeywell and "legally unsound").

Although the surrender of equivalents and intervening rights both involve a discussion of scope, the focus of these distinct inquiries differ. Google wholly ignores this distinction. For an intervening rights analysis, the focus is the scope of the new or amended claim. If the scope of the claim is substantively changed, e.g., narrowed, it gives rise to intervening rights. For a surrender of equivalents analysis, however, the "proper focus is whether the amendment narrows the overall scope of the claimed subject matter." Honeywell, 370 F.3d at 1141 (citing Festo, 535 U.S. at 736-37); id. at 1144. Indeed, the Federal Circuit in Honeywell expressly acknowledged that canceling an independent claim and rewriting a dependent claim in independent form gives rise to a presumptive surrender of equivalents, *even though* "*the scope of the rewritten claim has remained unchanged*." Id. at 1142 (emphasis added) (explaining that "the scope of subject matter claimed in the

independent claim" may nonetheless have been narrowed to secure the patent). This alone demonstrates that Honeywell cannot be extended in the manner urged by Google.

In short, the surrender of equivalents has no bearing on the scope of claim 16 for purposes of an intervening rights analysis. See, e.g., Safoco, 2009 WL 10742813, at *11 (finding that Honeywell "does not stand for the proposition that the surrender of equivalents through the operation of prosecution history estoppel changes the actual scope of claims rewritten in independent form, let alone that it changes them substantively for purposes of § 252"). "The limit on the range of equivalents that may be accorded a claim due to prosecution history estoppel is simply irrelevant to the interpretation of those claims." Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1578 (Fed. Cir. 1995) ("Claim interpretation in view of the prosecution history is a preliminary step in determining literal infringement, while prosecution history estoppel applies as a limitation on the range of equivalents if, after the claims have been properly interpreted, no literal infringement has been found."); see also Thermalloy, Inc. v. Aavid Eng'g, Inc., 121 F.3d 691, 694 (Fed. Cir. 1997) (holding that the doctrine of equivalents "has no place" in an analysis of whether amendments enlarged the scope of a claim for purposes of 35 U.S.C. § 305). The parties' remaining arguments—as to whether prosecution history estoppel should be found on the facts here—thus need not be reached. In view of the foregoing, claim 16 is not subject to the defense of intervening rights.

3. Accused Products

Absolute intervening rights apply to products that were made, purchased, used, or sold prior to the issuance of the reexamination certificate. Marine Polymer, 672 F.3d at 1362. Google demonstrates that accused products were purchased and/or used prior to the issuance of the '912 patent's reexamination certificate on February 8, 2021. Specifically, as to each of the five categories of accused products, Google sets forth data from purchase orders, financial records, and an internal database of its server fleet.

Based on the evidence presented, Google shows that (1) it stopped using 4-Rank DDR2 FBDIMMs by September 16, 2017, and thus, that entire category of accused products is subject

to absolute intervening rights; (2) it has not purchased 4-Rank DDR3 LRDIMMs or 4-Rank DDR4 NVDIMMs, and thus, these categories of accused products are moot; and (3) it purchased and used 4-Rank DDR4 RDIMMs, 4-Ranks DDR4 LRDIMMs, and server machines incorporating such technology prior to February 8, 2021, such that those products are subject to absolute intervening rights.

Netlist challenges the adequacy of Google's showing on three grounds. First, Netlist argues that February 8, 2021, the date the reexamination certificate issued, is not the critical date for this analysis. According to Netlist, the proper date is June 15, 2020, when the Federal Circuit affirmed the PTAB's decision. Netlist's argument is based on § 316(a), which provides that the PTO shall issue and publish a certificate of reexamination "when the time for appeal has expired or any appeal proceeding has terminated." As noted by Google, however, § 316(b) explicitly provides that intervening rights apply to products purchased or used "prior to the issuance of a [reexamination] certificate." See also Laitram, 163 F.3d at 1346 ("If substantive changes have been made to the original claims, the patentee is entitled to infringement damages only for the period following the issuance of the reexamination certificate."); P.J. Frederico, Commentary on the New Patent Act, 75 J. Pat. & Trademark Off. Soc'y at 206 ("the critical date is the date of the grant of the reissue").

Second, Netlist argues that Google has not disclosed in discovery all accused products. In particular, Netlist claims Google has withheld information on 8-Rank and 16-Rank DIMMs. Insofar as Google has withheld such information, Netlist should seek resolution of this issue before the magistrate judge assigned for discovery. At present, however, Netlist has only accused the five categories of 4-Rank DIMMs addressed in Google's motion. Google need not address products not presently at issue.

Third, Netlist argues that the evidence as to DDR4 RDIMMs and LRDIMMs is insufficient to show that the products were used or purchased in the United States or imported into the United States prior to February 8, 2021. Insofar as Netlist is arguing that products may have been purchased prior to February 8, 2021, but added to Google's inventory in the United States sometimes after that date, this is immaterial. Google provides evidence as to the date the

equipment was purchased, and such evidence is sufficient to establish a defense of intervening rights. BIC Leisure Prod., Inc. v. Windsurfing Int'l, Inc., 1 F.3d 1214, 1222 (Fed. Cir. 1993) (upholding district court's reliance on purchase orders). That Google also provides additional evidence simply bolsters its showing.

IV. MOTION TO AMEND

A. RELEVANT BACKGROUND

On February 12, 2010, Google filed an Answer and Counterclaim, alleging causes of action for: (1) Declaratory Judgment of Non-Infringement; (2) Declaratory Judgment of Invalidity; (3) Fraud/Deceit/Concealment; (4) Negligent Misrepresentation; and (5) Breach of Contract. Dkt. 18. As to its third, fourth, and fifth claims for relief, Google alleges that Netlist failed properly to disclose the '912 patent to JEDEC, thereby inducing others to rely on DDR standards as being free of intellectual property encumbrances.

As stated above, this was stayed on January 26, 2011 and reopened on February 17, 2021. On March 11, 2021, a scheduling order was issued setting deadlines for amended infringement and invalidity contentions, early briefing on the issue of intervening rights, and claim construction. No discovery deadlines were set. On September 3, 2021, an order issued staying discovery and vacating the deadlines for amended invalidity contentions and claim construction pending early resolution of the issue of intervening rights. On September 17, 2021, Google filed the instant motion to amend.

B. LEGAL STANDARD

A motion for leave to amend the pleadings generally is governed by Federal Rule of Civil Procedure 15(a). Where, as here, a pretrial scheduling order has been entered that sets a deadline to amend the pleadings and that deadline has passed, however, Rule 16(b) governs. Coleman v. Quaker Oats Co., 232 F.3d 1271, 1294 (9th Cir. 2000) (citing Johnson v. Mammoth Recreations, Inc., 975 F.2d 604, 607-08 (9th Cir. 1992)). Pursuant to Rule 16(b)(4), a scheduling order "may be modified only for good cause and with the judge's consent." Fed. R. Civ. P. 16(b)(4). "Good cause" may be shown where pretrial deadlines "'cannot reasonably be met despite the diligence of the party seeking the extension.'" Zivkovic v. S. Cal. Edison

Co., 302 F.3d 1080, 1087 (9th Cir. 2002) (quoting Johnson, 975 F.2d at 609). Although a court may consider prejudice to the opposing party, the "good cause" standard focuses primarily on the diligence of the moving party. In re W. States Wholesale Nat. Gas Antitrust Litig., 715 F.3d 716, 737 (9th Cir. 2013) (citing Johnson, 975 F.2d at 609). If diligence is not shown, the motion should be denied. Zivkovic, 302 F.3d at 1087 (citing Johnson, 975 F.2d at 609).

If good cause to modify the scheduling order is shown, the moving party must then demonstrate that leave to amend is warranted under Rule 15(a). Johnson, 975 F.2d at 608. Rule 15(a)(2) provides that a court "should freely give leave when justice so requires," and this policy is to be applied with "extreme liberality." Eminence Capital, LLC v. Aspeon, Inc., 316 F.3d 1048, 1051 (9th Cir. 2003). Courts consider five factors in determining whether to grant leave to amend: (1) undue delay; (2) bad faith or dilatory motive; (3) prejudice to the opposing party; (4) futility of amendment; and (5) repeated failure to cure deficiencies by amendments previously allowed. Id. at 1052 (citing Foman v. Davis, 371 U.S. 178, 182 (1962)). Of these factors, "it is the consideration of prejudice to the opposing party that carries the greatest weight." Id. "Absent prejudice, or a strong showing of any of the remaining Foman factors, there exists a *presumption* . . . in favor of granting leave to amend." Id. (emphasis in original).

C. DISCUSSION

Google moves for leave to amend its Answer and Counterclaim to add: (1) affirmative defenses of inequitable conduct and intervening rights; (2) a counterclaim for unfair competition; and (3) new facts in support of previously pled defenses and counterclaims of unclean hands, licensing, fraud, deceit, concealment, negligent misrepresentation, and breach of contract. Netlist does not oppose amendment to add new facts in support of previously pled defenses and counterclaims. The other proposed amendments are addressed below.

1. Intervening Rights

Google seeks to add the affirmative defense of absolute and equitable intervening rights. Good cause for this proposed amendment is clearly shown as the defense was unavailable before the reexamination proceedings. Netlist does not argue otherwise. Rather, Netlist argues that Google should not be permitted to amend its Answer to add an intervening rights defense

"generically." Opp'n at 14, Dkt. 212. Speculating that Google has failed to disclose certain classes of products, such as 8-Rank and 16-Rank memory modules, Netlist argues that Google should be required to allege its intervening rights defense as to the specific products it has disclosed and be foreclosed from asserting the defense as to any additional products it might be required to disclose in the future. This argument is not persuasive.

Netlist offers no evidence that Google has withheld pertinent discovery. But even if it had, this amounts to a discovery dispute that ought to be brought before the assigned magistrate judge. It has no bearing on whether Google should be permitted to allege an intervening rights defense in its Answer. The Complaint alleges that Google's infringing activities include its use of 4-Rank FBDIMMs; it does not identify any other class of product or purport to identify all classes of potentially infringing products. Google's Answer will not be required to provide more specificity than the pleading to which it responds. Accordingly, leave to amend to add the affirmative defense of absolute and equitable intervening rights shall be granted.

2. Inequitable Conduct

Google seeks to add the affirmative defense of inequitable conduct. Inequitable conduct requires that the patent applicant "misrepresented or omitted material information with the specific intent to deceive the PTO." Therasense, Inc. v. Becton, Dickinson and Co., 649 F.3d 1276, 1287 (Fed. Cir. 2011). Inequitable conduct must be pled with particularity under Rule 9(b). Exergen Corp. v. Wal-Mart Stores, Inc., 575 F.3d 1312, 1326 (Fed. Cir. 2009). Here, the inequitable conduct defense is premised on what Google alleges are contradictory statements Netlist made before the PTO during the reexamination proceedings and in this action. Specifically, in the reexamination proceedings, Netlist asserted that it had narrowed its claims to define its precise inventive contributions over the prior art, while in the instant action, Netlist asserts that those same amendments were merely clarifying. Good cause for this proposed amendment is clearly shown, as it could not have been asserted prior to Netlist making these statements. Netlist does not argue otherwise. Rather, it argues that the amendment is futile.

First, Netlist argues that attorney argument before the PTO is not a basis for inequitable conduct. "While the law prohibits genuine misrepresentations of material fact, a prosecuting

attorney is free to present argument in favor of patentability without fear of committing inequitable conduct." Rothman v. Target Corp., 556 F.3d 1310, 1328-29 (Fed. Cir. 2009) (citing Young v. Lumenis, Inc., 492 F.3d 1336, 1348 (Fed. Cir. 2007)). Google does not allege that Netlist misrepresented the substance of its amended claims or the relevant prior art. It alleges that Netlist mischaracterized claim amendments as narrowing. This may be the sort of attorney argument shielded from a claim of inequitable conduct. Nevertheless, attorney argument is not *per se* shielded; statements that fall "outside the bounds of permissible attorney argument" support a defense of inequitable conduct. Ring Plus, Inc. v. Cingular Wireless Corp., 614 F.3d 1354, 1360-61 (Fed. Cir. 2010) (rejecting patentee's claim that statement "was merely attorney argument and could not be a material misrepresentation"); ParkerVision, Inc. v. Qualcomm Inc., 924 F. Supp. 2d 1314, 1320 (M.D. Fla. 2013) (stating attorney argument may exceed the bounds of acceptability if it is based on distorted facts or contrary to what a person of ordinary skill in the art would understand). Based on the facts of this case, a determination whether Netlist's statement to the PTO constitutes a material misrepresentation or permissible attorney argument is best resolved at a later stage of the proceedings. See ParkerVision, 924 F. Supp. 2d at 1320 (declining to resolve issue on a motion to dismiss).

Netlist's other arguments are likewise unpersuasive. Netlist argues that Google fails to allege the requisite falsity. Relying on the different standards applicable in reexamination proceedings and infringement actions, Netlist asserts that an amendment can be narrowing under the BRI standard and clarifying under Phillips. However, falsity is a factual issue not properly resolved at the pleading stage. Netlist also argues that Google fails to show materiality because the PTAB did not expressly rely on Netlist's statement. The materiality standard, however, is objective. See Ring Plus, 614 F.3d at 1361 (rejecting claim that a misrepresentation of prior art was not material because the examiner did not cite to those references). Thus, for purposes of pleading, Google's allegations are sufficient. Finally, Netlist argues that Google has not alleged specific facts showing an intent to deceive. Google need not do so at this stage. Although inequitable conduct is subject to a heightened pleading standard, intent may be alleged generally, provided the pleadings allege sufficient underlying

facts from which a court may reasonably infer that a party acted with the requisite state of mind. Exergen, 575 F.3d at 1327 (citing Fed. R. civ. P. 9(b)). Accordingly, leave to amend to add the affirmative defense of inequitable conduct shall be granted.

3. UCL

Lastly, Google seeks to add a claim under California's unfair competition law ("UCL"), Cal. Bus. & Prof. Code § 17200 et. seq. Google clarifies in its reply brief that it seeks to state such a claim only under the UCL's fraud prong. To state a claim under that prong, Google must "allege facts showing that members of the public are likely to be deceived by the alleged fraudulent business practice." In re Anthem Inc. Data Breach Litig., 162 F. Supp. 3d 953, 990 (N.D. Cal. 2016). Here, Google alleges that Netlist failed to disclose in a timely fashion the '912 patent to JEDEC when the DDR standards were being considered and adopted. Courts have upheld UCL claims under similar circumstances. See Apple, Inc. v. Motorola Mobility, Inc., No. 11-CV-178-BBC, 2011 WL 7324582, at *11–14 (W.D. Wis. June 7, 2011) (denying motion to dismiss UCL claim where it was alleged that the patentee "ma[de] false licensing commitments to standards setting organizations" and "fail[ed] to disclose essential patents or applications to those organizations until after certain standards were adopted").

Google's claim is based on two separate allegations of fraud: (1) that Netlist failed to disclose in time the '912 patent (or the application for that patent) before JEDEC members voted to include the accused technology in the DDR2 and DDR3 standards; and (2) that Netlist failed to disclose the '912 patent at all before JEDEC members adopted the DDR4 standard. Regarding good cause, Google appears to acknowledge that the facts underlying the first instance of fraud were available prior to the issuance of the stay. Google notes that the same allegations underly its previously pled fraud claim, however; thus, Google is asserting only a new theory of liability, not new facts. As to the second instance of fraud, Google persuasively argues that the facts underlying this part of its UCL claim did not come to light until after the stay was lifted in this action, i.e., when Netlist amended its infringement contentions to allege that claim 16 of the '912 patent reads on DDR4 technology. Accordingly, good cause has been shown to allege the proposed UCL claim.

Regarding the propriety of amendment under Rule 15, Netlist argues that the UCL claim is futile on five grounds. First, Netlist argues that Google's UCL claim is barred by the four-year statute of limitations. As to the first instance of fraud set forth above (regarding the DDR2 and DDR3 standards), Google persuasively argues that the claim is permitted under the relation-back doctrine. As to the second instance of fraud, Google persuasively invokes the delayed discovery rule. See Robinson Helicopter Co. v. Dana Corp., 34 Cal. 4th 979, 990 (2004) (a fraud claim "is not deemed to have accrued until the discovery, by the aggrieved party, of the facts constituting the fraud or mistake"). Netlist allegedly failed to disclose the '912 patent as relevant to the DDR4 standards in or about September 2012. Google argues it was not on notice of Netlist's claim that DDR4 technology infringes the '912 patent, however, until Netlist served its amended infringement contentions in May 2021. Netlist counters that Google should have known the '912 patent applies to DDR4 technology because it is familiar with the patent, which "states on its face that it can apply to 'DDR1, DDR2, DDR3, and beyond.'" Opp'n at 5. However, a claim may be dismissed as barred by the statute of limitations only when the running of the statute is apparent on the face of the complaint. Von Saher v. Norton Simon Museum of Art at Pasadena, 592 F.3d 954, 969 (9th Cir. 2010). Given the allegations of the amended counterclaim, Google pleads facts to support delayed discovery.

Second, Netlist argues that Google has not alleged standing to sue under the UCL. A party has standing to sue under the UCL if it "suffered injury in fact" and "lost money or property as a result of the" challenged action. Cal. Bus. & Prof. Code § 17204. Economic injury may be shown in several ways, however, including being required to enter a transaction, costing money or property, that would otherwise be unnecessary. Ehret v. Uber Techs., Inc., 68 F. Supp. 3d 1121, 1133 (N.D. Cal. 2014). Google alleges, among other things, that it will be forced to pay Netlist exorbitant royalties due to the adoption of standards that did not account for Netlist's intellectual property. This is sufficient to allege standing.

Third, Netlist argues that Google's proposed amendment fails because it does not identify the prong or prongs of the UCL upon which it relies. Insofar as Google failed to do so

in its proposed amended counterclaim, however, it has now clarified that it alleges a claim solely under the fraud prong. Leave to amend will not be denied on this basis.

Fourth, Netlist argues that, to the extent Google bases its UCL claim on positions Netlist has taken in this litigation (i.e., that claim 16 covers certain embodiments of DDR4 technology), this is petitioning activity protected by the Noerr-Pennington doctrine and cannot serve as a basis for liability. Google's UCL claim is not premised on positions Netlist has taken in this litigation, however; it is premised on Netlist's failure timely to disclose the '912 patent to JEDEC. That Google learned of the patent's relevance to the DDR4 standard through Netlist's infringement contentions in this action does not mean the claim itself is based on those contentions. Rather, this simply alerted Google to the fact that Netlist should have disclosed the '912 patent as relevant to the DDR4 standard.

Fifth and finally, Netlist argues that Google fails to plead facts to state a UCL claim. To state a claim based on fraud, Google must plead facts showing that: (1) Netlist concealed or suppressed a material fact; (2) Netlist was under a duty to disclose the fact; (3) Netlist intentionally concealed or suppressed the fact with the intent to defraud; (4) Google was unaware of the fact and would have acted differently if it had known of the fact; and (5) as a result, Google sustained damages. Ahern v. Apple, Inc., 411 F. Supp. 3d 541, 561 (N.D. Cal. 2019). Google adequately alleges facts to support each element. It alleges that Netlist failed to disclose the '912 patent before JEDEC members voted on the relevant DDR standards; that Netlist was under a duty to disclose the patent pursuant to the JEDEC Patent Policy; that Netlist did so intentionally and with the intent to defraud; that the other JEDEC members including Google were unaware that the '912 patent was relevant to the DDR standards being voted upon, and that Netlist's silence induced them to rely on those standards as being free of intellectual property encumbrances; and that Google is now suffering damages as a result. No more is required. Accordingly, leave to amend to add a UCL counterclaim shall be granted.

V. CONCLUSION

As set forth above, it is hereby ordered that:

1. Google's motion to strike is granted in part and denied in part. The motion is granted with respect to the revised priority and conception dates set forth in Netlist's amended disclosures, and Netlist is precluded from asserting a priority or conception date earlier than July 5, 2004. The motion is denied with respect to the assertion of claim 16.

2. Google's motion for summary judgment on the issue of intervening rights is granted in part and denied in part. The motion is denied as to claim 16 and granted as to the remainder of the asserted claims (i.e., claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 34, 36-41, 43, 45-47, 50, 52-60, 62-65, 69-75, 77, and 80-91). As to these claims, accused products purchased and/or used prior to February 8, 2021 are subject to absolute intervening rights under 35 U.S.C. §§ 252 and pre-AIA 316(b).

3. Netlist's motion for summary judgment (i.e., that Google is not entitled to intervening rights as to claim 16) is granted.

4. Google's motion to amend its Answer and Counterclaim is granted.

5. This order terminates Docket Nos. 153, 155, 156, and 206.

6. The parties shall appear for a further case management conference on June 23, 2022 at 10:00 a.m. to be held via Zoom Webinar.

IT IS SO ORDERED.

Dated: May 5, 2022

Richard Seeborg
Chief United States District Judge

EXHIBIT B

Trials@uspto.gov
571-272-7822

Paper No. 13
Entered: May 5, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00063
Patent 10,217,523 B1

Before BRYAN F. MOORE, JON M. JURGOVAN, and SHEILA F. McSHANE, *Administrative Patent Judges.*

MOORE, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314(a)

I. INTRODUCTION

A. Background

Samsung Electronics Co., Ltd. ("Petitioner")[1] filed a Petition requesting *inter partes* review of claims 1–34 ("the challenged claims") of U.S. Patent No. 10,217,523 B1 (Ex. 1001, "the '523 patent") pursuant to 35 U.S.C. §§ 311–319, along with the supporting Declaration of Dr. Vivek Subramanian. Paper 1 ("Pet."); Ex. 1003. Netlist, Inc. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 7 ("Prelim. Resp."). With authorization (Paper 8), Petitioner filed a Reply to Patent Owner's Preliminary Response (Paper 11 ("Pet. Reply")), with Patent Owner filing a Sur-Reply (Paper 12 ("PO Sur-Reply")).

We have authority under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons that follow, we determine that Petitioner has demonstrated that there is a reasonable likelihood that it would prevail in showing the unpatentability of at least one of the challenged claims. For the reasons set forth below, and pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1–34 of the '523 patent.

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[1] Petitioner identifies itself and Samsung Semiconductor, Inc. as another real party-in-interest. Pet. 1.

B. Related Proceedings

At the time of the Petition filing, Petitioner indicated *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.,* No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021) ("Related Case") involves the '523 patent. Pet. 1. Petitioner also identified several other related matters. Pet. 1–3. At the time of the filing of Mandatory Notices, Patent Owner also identified several related matters. Paper 5, 3–5 (Notices).

The Board previously instituted trial in IPR2020-01421 on the same claims of the '523 Patent and on the same grounds presented here, but with a different petitioners, SK hynix Inc. and SK hynix America Inc. *See* Ex. 1043. That IPR was terminated after institution because a settlement was reached. Ex. 1044.

C. The '523 Patent

The '523 patent is titled "Multi-Mode Memory Module with Data Handlers" and issued on February 26, 2019, from an application filed on March 29, 2014. Ex. 1001, codes (22), (45), (54).

The '523 patent is directed to a self-testing memory module for testing a plurality of memory devices mounted thereon. Ex. 1001, 5:4–27. Figure 2, reproduced below, is a block diagram illustrating component blocks of memory module 12 and memory controller 14. Ex. 1001, 5:28–34, 8:41–62, 9:22–42, Fig. 2.

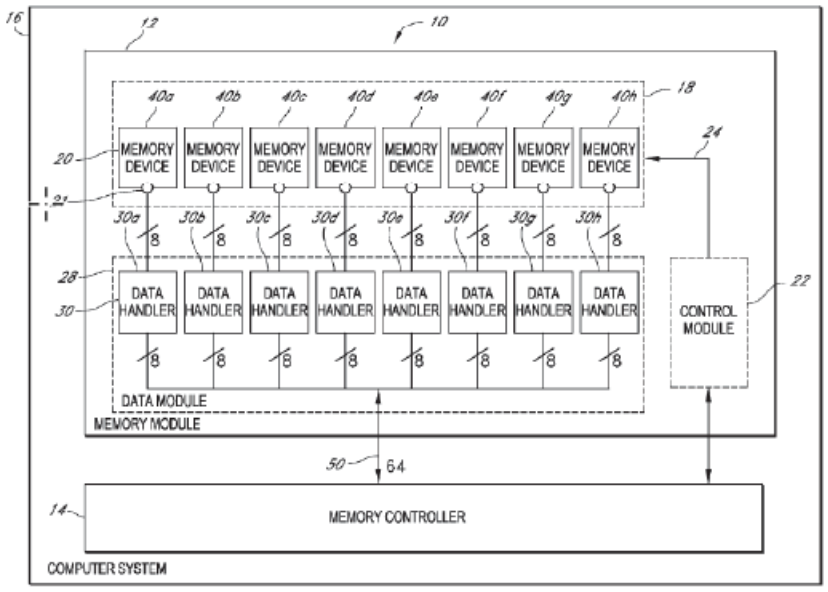


FIG. 2

Figure 2, above, shows memory module 12 includes control module 22 that generates address and control signals for testing memory devices 20 and data module 28 that includes a plurality of distributed data handlers 30 that are each located in proximity to corresponding memory device 20 and act as a buffer between memory device 20 and system memory controller 14. Data handlers 30 of data module 28 generate test patterns to write to memory devices 20 and compare test patterns read from memory devices 20 to the written patterns to identify faults. *Id.*

Figure 3, reproduced below, provides additional detail regarding the control module, data handlers and their components and interconnections. Ex. 1001, Fig. 3.

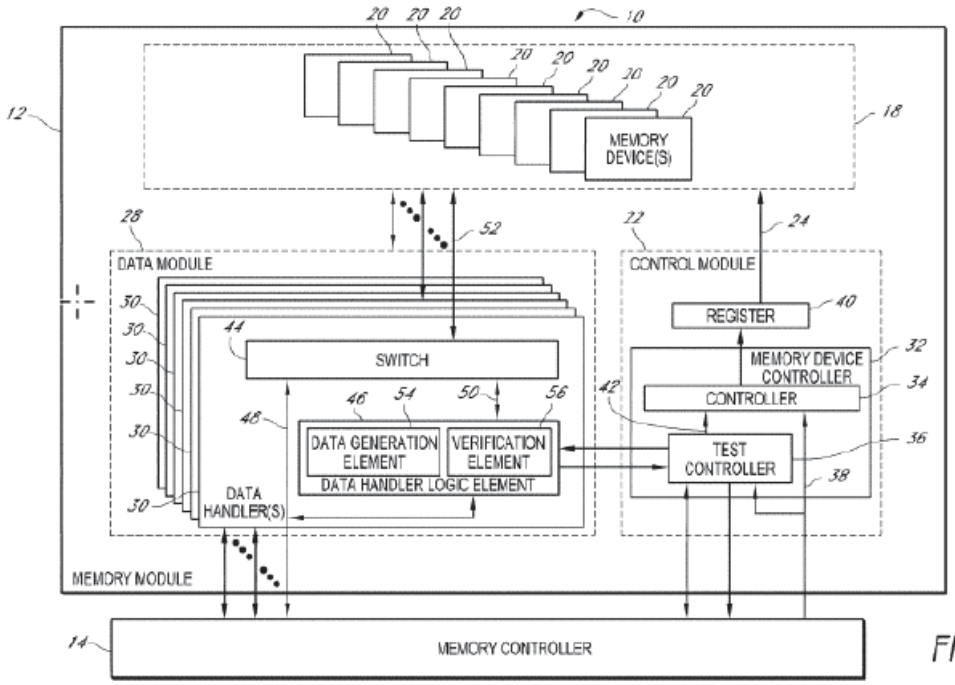


FIG. 3

As shown in Figure 3, above, shows additional control module 22, data handlers 30, and memory devices 20 and certain components thereof.

Challenged claims 1 and 19 of the '523 patent are independent. Claim 1, an illustrative independent claim of the '523 patent, is reproduced below, with sub-paragraphing added to the limitations for reference purposes.

> 1. [a] A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:
>
> [b] memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;
>
> [c] a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements;
>
> [d] a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and

> [e] wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;
>
> [f] [i] wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and [ii] the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, [iii] the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and
>
> [g] [i] wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and [ii] the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and [iii] wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.

Ex. 1001, 16:55–17:30.

D. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–34 of the '523 patent on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)
1–34	103(a)	Ellsberry,[2] Jeddeloh[3]

[2] US Pub. No. 2006/0277355 A1, published December 7, 2006. Ex. 1005.

Claims Challenged	35 U.S.C. §	Reference(s)
1–34	103(a)	Ellsberry, Jeddeloh, Averbuj[4]
14, 17–34	103(a)	Ellsberry, Jeddeloh, Lee[5]
14, 17–34	103(a)	Ellsberry, Jeddeloh, Averbuj, Lee

Pet. 5.

II. DISCRETIONARY DENIAL UNDER § 314(a)

A. Overview

Patent Owner requests that we exercise our discretion under 35 U.S.C. § 314(a) to deny the Petition under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"). Prelim. Resp. 43–45.

In assessing whether to exercise such discretion, the Board weighs the following factors:

> 1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
>
> 2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
>
> 3. investment in the parallel proceeding by the court and the parties;
>
> 4. overlap between issues raised in the petition and in the parallel proceeding;
>
> 5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
>
> 6. other circumstances that impact the Board's exercise of discretion, including the merits.

---

[3] US 7,310,752 B2, issued December 18, 2007, claiming priority to Application No. 10/660,844, filed on Sept 12, 2003. Ex. 1006.
[4] US Pub. No. 2005/0257109 A1, published November 17, 2005. Ex. 1007.
[5] US Pub. No. 2006/0095817 A1, published May 4, 2006. Ex. 1008.

Fintiv at 6. Recognizing that "there is some overlap among these factors" and that "[s]ome facts may be relevant to more than one factor," the Board "takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Id.*

As identified above, the Related Case, which is a declaratory judgment action involving the '523 patent, is pending in the District of Delaware. *See* Prelim. Resp. 44.

We address each *Fintiv* factor below.

B. Factor 1 – Stay of Related Litigation Proceeding

Patent Owner asserts a stay is unlikely given that an IPR against another patent asserted in the Related Case was filed within a week of the Preliminary Response. *Id.* We decline to attempt to predict how the District Court would proceed should a stay be requested by either of the parties. Accordingly, we find that this factor neither favors nor weighs against discretionary denial of *inter partes* review.

C. Factor 2 — Proximity of Court's Trial Date

Patent Owner admits that "[t]he district of Delaware has not yet set a trial date." *Id.* Accordingly, this factor weighs against exercising our discretion to deny *inter partes* review.

D. Factor 3 — Investment in the Parallel Proceeding

Patent Owner admits "[t]he parties have invested in pleading and motion practice in the parallel proceeding, although claim construction and merits determinations have not been reached." *Id.* at 44–45. Accordingly, in view of the significant work that remains to be completed in the Related Case, this factor weighs against exercising our discretion to deny *inter partes* review.

E. Factor 4 — Overlap With Issues Raised in Parallel Proceeding

Patent Owner admits that "Petitioner does not challenge the validity of the '523 Patent in the parallel proceedings." *Id.* at 45. Nevertheless, "Petitioner has agreed to a *Sotera*-type stipulation to avoid any overlap with the Delaware action . . . ." Pet. Reply 2. Consequently, we find that this factor weighs against exercising our discretion to deny *inter partes* review.

F. Factor 5 — Commonality of Parties in Parallel Proceedings

Patent Owner asserts that the Petitioner is a party to the Related Case. Prelim. Resp. 45. In *Huawei Tech. Co. v. WSOU Inv., LLC*, IPR2021-00225, the Board found "this factor favors denial if trial precedes the Board's Final Written Decision and favors institution if the opposite is true." Paper 11 at 14 (PTAB June 14, 2021) (internal quotation marks omitted). Given that no trial date has been set in the Related Case, we find that this factor weighs against exercising our discretion to deny *inter partes* review.

G. Factor 6 — Other Circumstances

Patent Owner argues that we should consider that the "Petitioner here has not met its burden of showing that the asserted prior art and/or arguments were not already considered by the Office in the '523 Patent's prosecution, much less demonstrated a material error by the Office." *Id.* Those issues are more relevant to an evaluation of discretionary denial under 325(d). Thus, this factor is neutral.

H. Conclusion

The *Fintiv* factors weigh strongly against exercising our discretion to deny *inter partes* review. Thus, based on our holistic assessment of the *Fintiv* factors, we decline to exercise our discretion under 35 U.S.C. § 314(a) to deny *inter partes* review.

III. DISCRETIONARY DENIAL UNDER § 325(d)

Patent Owner contends that we should deny institution under 35 U.S.C. § 325(d) because the Petition reuses the same art and arguments that were previously presented to the Office. Prelim. Resp. 41. Patent Owner asserts "Petitioner has the burden to establish why the art and proposed grounds present something *new* and *nonduplicative* of what was before the Office during prosecution, yet failed to do so." *Id.* at 42. Specifically, Patent Owner argues "Petitioner has not shown that Ellsberry, Jeddeloh, or the arguments based thereon, are not substantially the same as the art and arguments the Office considered during prosecution, and Averbuj was even expressly considered and made of record during prosecution." *Id.* at 42–43. Petitioner argues that we should not exercise discretion under § 325(d) to deny institution because Petitioner does not have any specified burden under § 325(d) and "during prosecution the Examiner specifically complained about the 'unreasonable' number of prior-art references that Patent Owner was dumping into the record without any explanation of their relevance." Pet. Reply. 1–2 (citing Ex. 1002, 226).

Applicable Framework

Pursuant to 35 U.S.C. § 325(d), the Director may elect not to institute a proceeding if the challenge to the patent is based on matters previously presented to the Office. Section 325(d) states, in relevant part, "[in] determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." The Board

uses the following two-part framework in determining whether to exercise discretion under § 325(d) to deny institution:

> (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 3, 2020) (precedential).

In applying the two-part framework, we consider the following non-exclusive factors:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph). Factors (a), (b), and (d) relate to whether the art or arguments presented in the Petition are the same or substantially the same as those

previously presented to the Office. *Advanced Bionics*, Paper 6 at 10. Factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office. *Id.* If a condition of the first part of the framework is satisfied and the petitioner fails to make a showing of material error, the Director generally will exercise discretion not to institute *inter partes* review. *Advanced Bionics*, Paper 6 at 9.

As to the burden, Patent Owner argues "Petitioner *always* 'has the burden from the onset to show with particularity why the patent it challenges is unpatentable' ***and why the Office should use its discretion to institute***. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363, 1367 (Fed. Cir. 2016); 35 U.S.C. § 312(a)(3) [("*Harmonic*")]; *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (no burden on patent owner) [("*Drinkware*")]." Nevertheless, neither *Drinkware* nor *Harmonic* discusses or professes to address whether the burden on Petitioner with regard to its patent challenge applies to the Board's ability to deny institution for discretionary reasons. We find that the second part of the *Advanced Bionics* test requires that Petitioner point out sufficiently how the Examiner erred;[6] however, the first part of the *Advanced Bionics* test does not assign a specific burden or responsibility on Petitioner to initially disprove that the same or substantially the same art at issue was previously presented to the Office. Thus, we disagree with Patent Owner that "Petitioner has the burden to establish why the art and proposed grounds present something *new* and *nonduplicative* of what was before the Office during prosecution." *See* Prelim. Resp. 42.

[6] We do not need to decide here if this is correctly characterized as a "burden."

Relevant Procedural History

The Averbuj reference asserted in the IPR was cited in an IDS during prosecution of the '523 patent. Ex. 1002, 61, 255. We do not find, and Patent Owner does not cite to, any substantive discussion of Averbuj in the prosecution history.

Part One of Advanced Bionics Framework

In the first part of the *Advanced Bionics* framework, we consider whether the same or substantially the same art or arguments previously were presented to the Office. *Advanced Bionics*, Paper 6 at 8. *Becton, Dickinson* factors (a), (b), and (d) inform the analysis. *Id.* at 9–10.

Patent Owner contends that Averbuj was expressly considered during prosecution of the '523 patent. Prelim. Resp. 42. As noted above, Averbuj was submitted in an IDS. Ex. 1002, 61, 255. During prosecution, the Examiner stated "[i]t is unreasonable for Examiner to review all of the cited references thoroughly" and that "only a cursory review [of the cited references] has been made." Ex. 1002, 226.

Given the facts above, because Averbuj was not presented in combination with the other references asserted here and is only used in two of the four grounds, the combination of references asserted in the Petition do not qualify as art that was "previously presented" to the Office. Thus, we find that the combination of references asserted in the Petition, were not previously presented to the Office.

Additionally, Patent Owner does not assert or explain sufficiently that Ellsberry, Jeddeloh, and/or Lee are cumulative of any reference cited during prosecution of the '523 patent. Prelim. Resp. 41–43. On this record, we are

not persuaded that Ellsberry, Jeddeloh, and Lee are cumulative of any reference cited during prosecution of the '523 patent.

Accordingly, the first condition of the first part of the *Advanced Bionics* framework is not satisfied, and we need not consider whether Petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Conclusion

After evaluating the *Becton, Dickinson* factors within the *Advanced Bionics* framework, and based on the particular circumstances here, we conclude that the combination of references asserted in the Petition, were not previously presented to the Office. Thus, the same or substantially the same prior art as in the Petition was not presented previously to the Office. Accordingly, we determine that discretionary denial of the Petition under 35 U.S.C. § 325(d) is not appropriate.

IV. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have a "Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST." Pet. 6.

Patent Owner does not dispute Petitioner's characterization or offer its own. Accordingly, for purposes of this decision, we adopt Petitioner's characterization of the level of ordinary skill, which we determine is consistent with the '523 patent written description and the asserted prior art.

B. Claim Construction

For cases like this one, where the petition for *inter partes* review was filed after November 13, 2018, the Board interprets claim terms in accordance with the standard used in federal district court in a civil action involving the validity or infringement of a patent. *See* 37 C.F.R. § 42.100(b) (2019). Under the principles set forth by our reviewing court, the "words of a claim 'are generally given their ordinary and customary meaning,'" as would be understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic*, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1015, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner offers constructions of several terms which are not disputed by Patent Owner. Pet. 13–15. Nevertheless, we determine that it is not necessary to provide an express interpretation of any of the terms of the claims at this juncture. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.").

C. Legal Background

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.[7] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Alleged Obviousness of Claims 1–34 Over Ellsberry and Jeddeloh

Petitioner contends that claims 1–34 are rendered obvious by the combination of Ellsberry and Jeddeloh. Pet. 34–96. To support its contentions, Petitioner provides explanations as to how Ellsberry and Jeddeloh teach each claim limitation. *Id.* Petitioner also relies upon the Subramanian Declaration (Ex. 1003) to support its positions. Patent Owner presents no issues or arguments specific to reading the teachings of references on the limitations, rather Patent Owner concentrates its disputes on the motivation to combine the prior art and alleges hindsight in the combination. *See generally* Prelim. Resp. Patent Owner also relies upon the Brogioli Declaration (Ex. 2001) to support its positions.

[7] Patent Owner presents no objective indicia in the Preliminary Response. *See generally* Prelim. Resp.

We begin our discussion with a brief summary of Ellsberry and Jeddeloh and then address the evidence and arguments presented.

1. Ellsberry (Ex. 1005)

Ellsberry relates to "a device, system, and method for expanding the memory capacity of a memory module." Ex. 1005, code (57). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry, shown below, "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." Ex. 1005 ¶ 28. System 200 has DIMM interface 202 that couples to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted. *Id.* The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206, 208. *Id.*

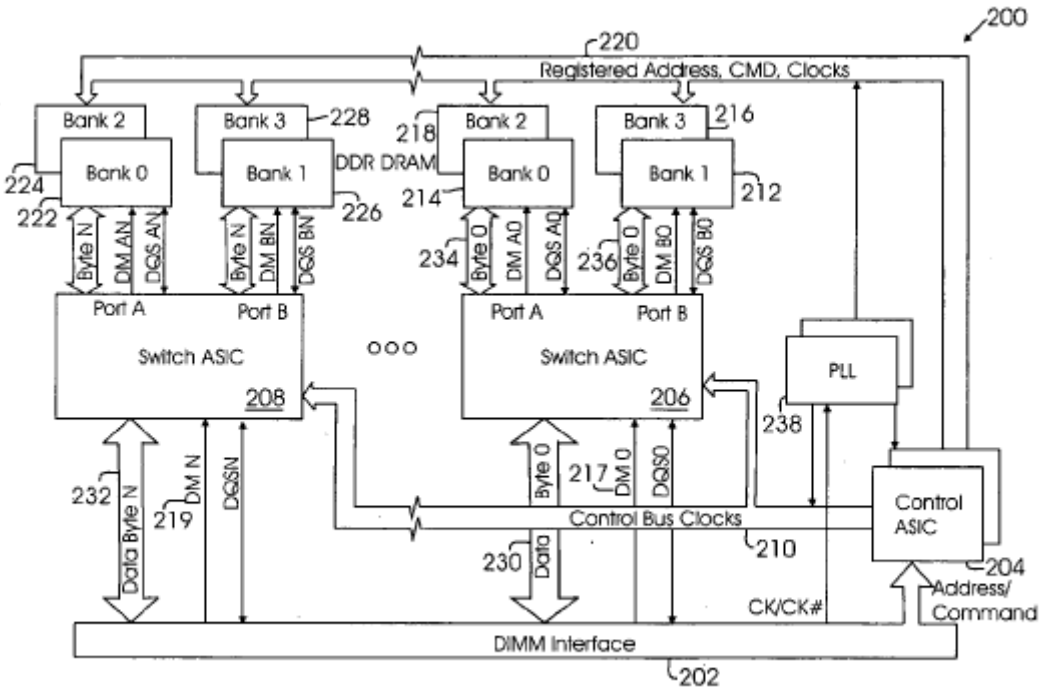


Fig. 2

Figure 2, above, illustrates a block diagram of a capacity-expanding memory device.

Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. Ex. 1005 ¶¶ 28–29.

Specifically, control unit 204 receives memory addresses and commands from DIMM interface 202 and controls switches 206 and 208 via control bus 210 to indicate how data from DIMM interface 202 should be received from and/or stored in memory banks 212–228. Ex. 1005 ¶¶ 29–30, Fig. 2. Control unit 204 also generates address and command information on address bus 220 to access memory banks 212–228. *Id.* Switches 206 and

208 receive data from, or provide data to, DIMM interface 202 via data buses 230 and 232. *Id.*

2. Jeddeloh (Ex. 1006)

Jeddeloh relates to "[a] memory module [that] includes several memory devices coupled to a memory hub [that] includes several link interfaces coupled to . . . a self-test module." Ex. 1006, code (57). Jeddeloh's Figure 3, reproduced below, depicts each of the following self-test elements as a "functional block," teaching that each block is "conventional, and can be implemented using well-known techniques and circuitry" (*id.* at 9:46–51):

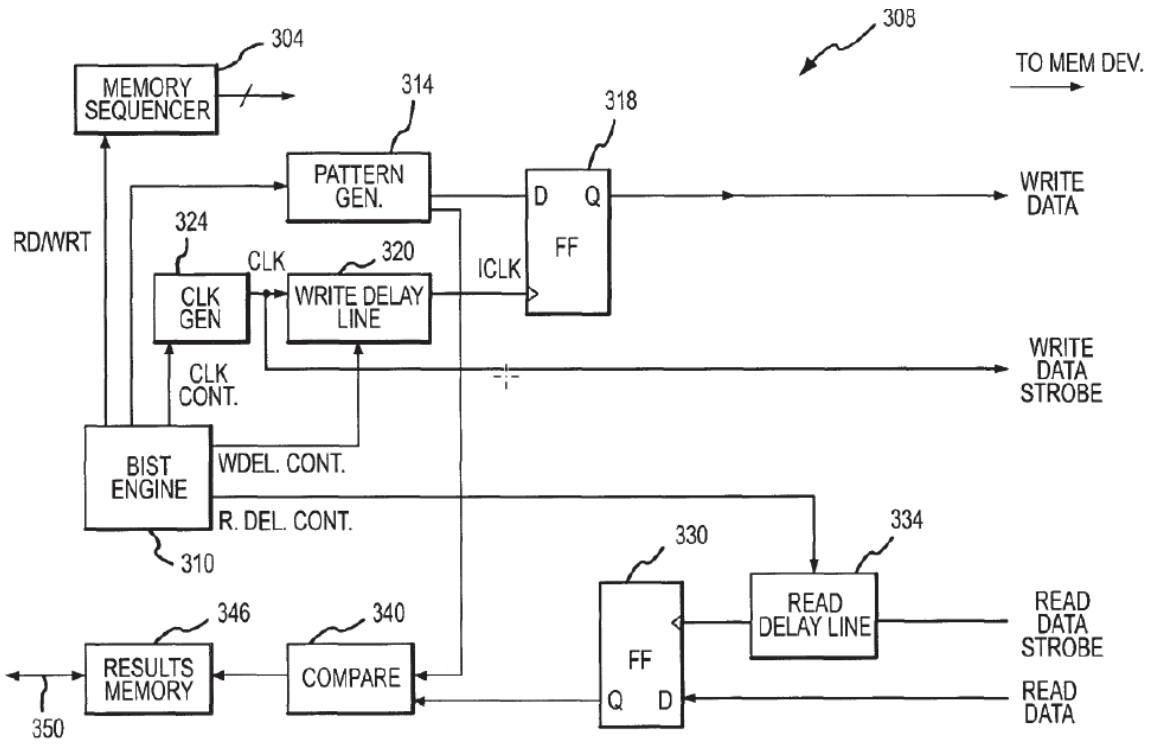


FIG.3

Figure 3, above, illustrates a block diagram of a self-test device.

Figure 3 above, shows BIST engine 310 and memory sequencer 304 that generate and distribute address and command/control signals during testing, and pattern generator 314, compare circuit 340, and results memory 346 that generate, distribute, and compare test patterns, and store fault information. *Id.* at 9:57–67, 10:30–51. Jeddeloh also discloses use of a SMBus to communicate with off-module components, for instance, a test apparatus can use it to "set memory testing parameters and receive test results." *Id.* at 8:26–53, 10:47–51.

2. Analysis

a. Motivation to Combine

Petitioner contends it would have been obvious to modify the teachings of Ellsberry with Jeddeloh's teachings to include self-test functionality. Pet. 25–34. As background to the discussion motivation to combine, below we discuss Petitioner's proposed combination of Ellsberry and Jeddeloh.

Ellsberry discloses a memory module that separates circuitry into handling address and control signals and handling data signals as represented in Petitioner's annotated Figure 2 below. Pet. 27 (citing Ex. 1005, Fig. 2).

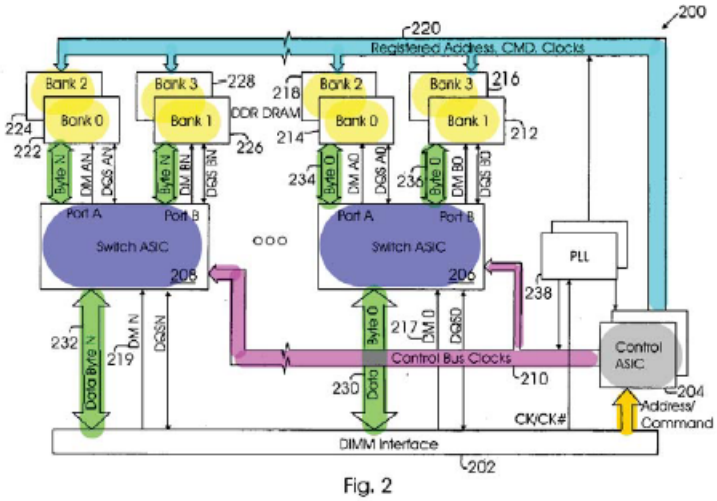


Fig. 2

Petitioner's annotated Figure 2 of Ellsberry above shows address/control signals are handled by Control ASIC 204 (grey) and data signals are handled by a plurality of distributed Switch ASICs 206 thru 208 (purple). *Id.* at 26–27. Jeddeloh discloses a "functional block diagram" of self-test circuitry in Figure 3 (annotated). *Id.* at 29 (citing Ex. 1006, Fig. 3).

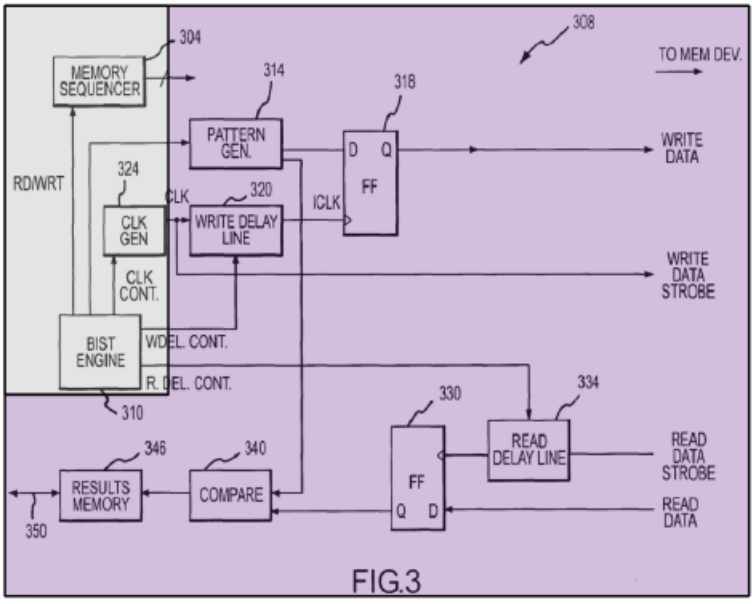
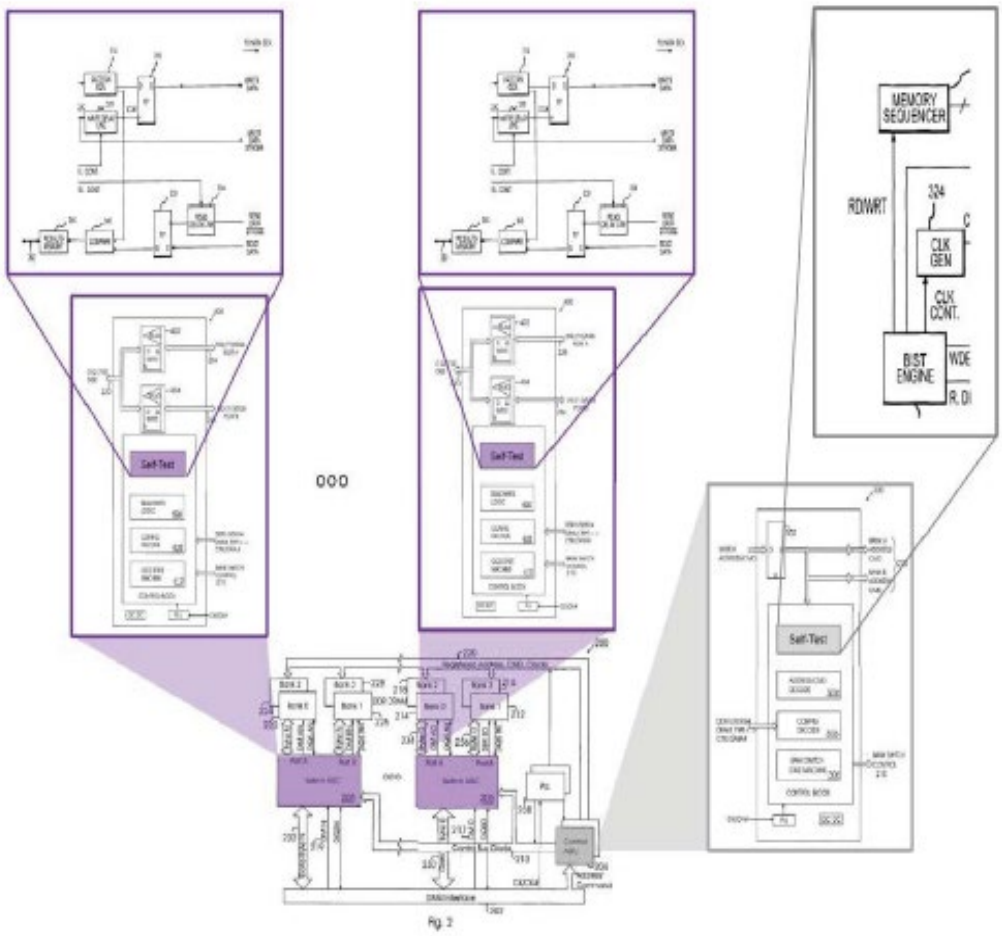


FIG.3

Petitioner's annotated Figure 3 above shows a BIST engine 310, clock generator 324, and memory sequencer 304 (in grey) that generate and distribute address and command/control signals during testing, and pattern

generator 314, compare circuit 340, and results memory 346 (in purple) that generate, distribute, and compare test patterns, and store fault information. *Id.*

In Petitioner's combination, the self-test functionality of Jeddeloh would be divided between circuitry for handling address/control signals and circuitry for handling data signals. Self-test address/control signal circuitry would be implemented in Ellsberry's Control ASIC to send commands to self-test data signal circuitry implemented in Ellsberry's distributed Switch ASICs and address and control information to the memory devices in order to carry out the testing functionality described in Jeddeloh. *Id.* at 29–30. This combination is represented by Petitioner's annotated combination of Figure 2 of Ellsberry and Figure 3 of Jeddeloh, reproduced below. *Id.* at 30 (citing Ex. 1006, 9:46–51, Fig. 3).



As represented in Petitioner's annotated combination of Figure 2 of Ellsberry and Figure 3 of Jeddeloh, above, to carry out self-test functionality, the self-test circuitry in the modified Control ASIC would send address/control signals to the memory devices (*e.g.*, over the bus of Ellsberry Figure 2) and command signals to the Switch ASICs (*e.g.*, over bus 210 of Ellsberry Figure 2), as Petitioner contends is taught by Ellsberry and Jeddeloh. *Id.* at 30–31 (citing Ex. 1005 ¶ 56, Fig. 13; Ex. 1006, 10:30–51; Ex. 1003 ¶ 143). Additionally, to enter test mode and carry out the self-test functionality, the memory module would first receive mode commands (e.g., over a maintenance bus), as Petitioner contends is taught by Jeddeloh. *Id.* (citing Ex. 1006, 8:26–53, 10:3–6).

For purposes of this Decision, and based on Petitioner's citations to specific prior art disclosures and supporting evidence, we are persuaded that Petitioner sets forth sufficient articulated reasoning with rational underpinning to support the legal conclusion that it would have been obvious to modify the teachings of Ellsberry with Jeddeloh's teachings to include self-test functionality. *Id.* at 31–37. For example, Petitioner asserts:

> Ellsberry and Jeddeloh[] are analogous art to the 523 Patent because each is in the same field of endeavor – memory module design and architecture, EX1001, 1:32-33; EX1005, Abstract; EX1006, 3:61-4:19, and each is reasonably pertinent to the 523 Patent's addressed problem – improving memory modules by architecture design and/or testing, EX1001, 1:32-33; EX1005, Abstract; EX1006, 3:61-4:19. EX1003, ¶145.
>
> Also, a Skilled Artisan would have considered the Combined System to be an arrangement of old elements each performing its known functions (Ellsberry's module acting as computer storage and Jeddeloh[]'s self-test functionality performing self-test on that module) and yielding what one would expect from the arrangement (a memory module with self-test). Ellsberry and Jeddeloh[] each employ known signaling and testing techniques found in many prior art systems. EX1006, 9:46-51. Combining them would therefore have been well within a Skilled Artisan's abilities, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. EX1003, ¶¶146-147.

Id. at 31–32.

Additionally, as to why a testing mode would be added to Ellsberry, Petitioner contends there are several specific reasons ("Reasons for Testing"). *Id.* at 32–34; Ex. 1003 ¶¶ 149–53. For example, Petitioner first contends, quoting a non-asserted reference, that "[a]s chips become faster in frequency, there is a greater need for hardware to include self-test logic." *Id.*

at 32 (citing Ex. 1018, 1:14–18). Thus, Petitioner contends that Ellsberry discloses that its modules are JEDEC compliant and JEDEC standards at the time required self-testing. *Id.* (citing Ex. 1005 ¶ 50, claims 10, 19; Ex. 1016, 1–2, 25–28, 55–66; Ex. 1017, 2–11). Second, Petitioner contends that because Ellsberry's Control ASIC configures the memory devices on the module "rather than [being] directly programmed by the host system," a person of ordinary skill would have been motivated to have a built in testing capability in the Control ASIC itself. *Id.* at 33 (citing Ex. 1005 ¶ 44; Ex. 1003 ¶ 150). Third, Petitioner contends that Jeddeloh emphasizes the need for testing circuitry in memory modules because of the increasing significance of signal timing. *Id.* (citing Ex. 1006, 2:41–51, 3:47–52). Fourth, Petitioner contends that because Ellsberry describes that its Control ASIC configures the memory devices, one of ordinary skill would be motivated to add testing and, further, because Ellsberry has a "Mode pin," to operate in other modes, a skilled artisan would have been motivated to provide functionality to switch between additional modes. *Id.* at 33–34 (citing Ex. 1005 ¶ 33; Ex. 1003 ¶ 152). Fifth, Petitioner also contends "a Skilled Artisan would have been motivated to add testing in a mode separate from normal operating mode because the purpose of testing was to confirm the module would operate appropriately in normal mode." *Id.* at 34 (citing Ex. 1006, 2:43–50, 3:47–53; Ex. 1016, 1–2, 25–28 55–66; Ex. 1017, 2–11. Ex. 1003 ¶ 153). Sixth, Petitioner would add testing mode because "normal operation where the host sends read/write commands to the Control ASIC would interfere with such testing." *Id.*

Finally, as to the motivation to distribute Jeddeloh's components into different parts of Ellsberry, Petitioner contends there are several reasons, including:

- First, such distribution is consistent with Ellsberry's architecture. (Pet. 35);

- Second, such a distribution of self-test functionality is consistent with how each of Ellsberry's Switch ASICs already included logic elements and connections for implementing data transactions in 8-bit portions (Pet. 35–36);

- Third, a Skilled Artisan would have been motivated to make such a design because other references teach Skilled Artisans to place such self-test functionality in distributed data buffers similar to Ellsberry's Switch ASICs (Pet. 36 (citing Ex. 1019 ¶¶ 77, 97, Figs. 5, 18; Ex. 1020, 15:57–65, 18:63–19:23, 35:10–37:1, Figs. 5, 18, 36; Ex. 1007 ¶¶ 49–50, 53, 55–57, Figs. 1, 6–7; Ex. 1025, 30));

- Fourth, an additional reference, Lepejian, teaches Skilled Artisans that, in order to reduce busing area, pattern generators should be distributed to each of the Switch ASICs. (Pet. 36 (citing Ex. 1021, 3:45–53));

- Fifth, "a Skilled Artisan would have been motivated to place self-test pattern generator functionality, such as Jeddeloh[]'s, in Ellsberry's Switch ASICs in order to place it close to its associated memory devices, thereby simplifying the wiring plan on the circuit board" (Pet. 36–37); and

- Sixth, quoting another reference, Zimmerman, it was known that "functionality shown embodied in a single integrated circuit or functional block may be implemented using multiple cooperating circuits or blocks, or vice versa." (Pet. 37 (citing Ex. 1026, 7:43–46, Ex. 1027, 7:7–14)).

Pet. 34–37; Ex. 1003 ¶¶ 154–65.

In response, Patent Owner argues that Ellsberry fails to disclose the claimed "second mode" [or testing mode], as recited in claims 1 and 19, because it would not have been obvious to one of ordinary skill in the art to modify Ellsberry to provide for the "second mode." Prelim Resp. 10. Specifically, Patent Owner argues

> First, the Petition fails to show that a POSITA would have been motivated in the first place to combine Ellsberry, which is directed to memory emulation, with Jeddeloh, which is directed to a central hub architecture with separate self-test module. EX2001, ¶¶39-44. Second, a POSITA would not disassemble parts of Jeddeloh's self-test module and distribute it across the Ellsberry's memory module architecture because doing so directly conflicts with, and is taught away by, the teachings of both Ellsberry and Jeddeloh. EX2001, ¶¶45-58. Finally, the Grounds fail because the Combined System is not functional as proposed, and modifying the proposed combination so that would have functioned in the manner required by the claims would have been beyond the technical ability of a POSITA. EX2001, ¶¶ 59-69.

Id.; *see also id.* at 11–40. As explained below, in general, these arguments do not sufficiently undermine Petitioner's contentions but, in some instances, we determine that these issues are better resolved during trial.

More specifically, Patent Owner argues "Petitioner proposes that the centralized self-test module of Jeddeloh be disassembled and spread across different circuits within Ellsberry. However, the architectures of Ellsberry and Jeddeloh are antithetical to one another, and a POSITA would not have found it obvious to combine them or have known how to accomplish such a feat." Prelim. Resp. 25.

Patent Owner asserts that "the references [cited by Petitioner's declarant] show what a POSITA could have done, but do not show or teach

that said POSITA would have actually been motivated to redundantly distribute parts of Jeddeloh's architecture across Ellsberry's switch ASIC." Prelim. Resp. 30.

Patent Owner argues that "in order to create a ***functional*** switch ASIC [] Petitioner further alleges (without pointing to any particular reference) that a POSITA would have implemented a MUX/DEMUX circuit in order to manage the data convergence resulting from Ellsberry's originally-disclosed data paths and Petitioner's newly-concocted data path." *Id.* at 21. Patent Owner further argues "the architectures of Ellsberry and Jeddeloh are antithetical to one another" because for example, "Jeddeloh's self-test module is placed *behind* (relative to memory devices) its memory interface components," as opposed to in "new data paths between the memory controller and the memory devices in Ellsberry" as in Petitioner's combination. *Id.* at 25, 29. Specifically, Patent Owner explains "Jeddeloh's self-test module needs Jeddeloh's memory interface components to ensure that the nature of the signals sent and received by memory controller 280 correspond to the nature of the signals that memory devices are capable of sending and receiving." *Id.* at 29. Patent Owner also argues "Petitioner wholly ignores the fact that Jeddeloh's self-test module ***requires*** its memory interfaces to interact with memory devices, and provides no explaining how a POSITA would include said memory interfaces into Ellsberry. Ultimately, Patent Owner asserts "this combination alone would not have resulted in an operable system, and a POSITA would not have had the technical skill to make it operable without undue experimentation." *Id.* at 24.

Patent Owner also relies on U.S. Patent No. 8,154,901 (the '901 patent) for the proposition that adding a multiplexer would "present

transmission line discontinuity regions in electronic systems (e.g., in electronic systems with signal paths with electrical lengths longer than ¼ of the wavelength of the operational frequency or the signal transition rate)" and "signal reflections may occur, changing wave characteristics and degrading system performance." *Id.* at 33–34 (citing Ex 2002, 1:40–56). Thus, Patent Owner's argument focuses on motivation to combine, teaching away, and the ability of one of ordinary skill to make the combination.

Petitioner contends "in the Combined System data travels over two different data paths in the two different modes. Because each path merges into the same port on the Switch ASIC, only one path can be used at a time, using for instance a MUX/DEMUX as was well-known, otherwise there could be data collisions." Pet. 59 (citing Ex. 1003 ¶ 242).

Petitioner cites to its declarant who testifies extensively on how the combined system could be implemented and relies on several non-asserted references as support for that testimony. Ex. 1003 ¶¶ 258–59 (citing Exs. 1006, 1007, 1026, 1035, 1030 (pin citations omitted)).

Although we find that Petitioner has provided sufficient evidence in support of the proposed combination at this juncture, the parties' evidence, particularly the declarants' testimony, presents a classic battle of the experts, which we determine would be more fully addressed during a trial. Patent Owner and Petitioner will have the opportunity to cross-examine Dr. Subramanian and Dr. Brogioli, respectively, during the course of the trial.

As such, we invite the parties to further address the combination of references during the trial. For example, the parties should address the issue of whether the new data paths created with Jeddeloh's self-test module

placed behind (relative to memory devices) its memory interface components would have been within the ability of one of ordinary skill to achieve. Although this issue was raised in IPR2020-01421, the instant Petitioner here, Samsung Electronics, has not had the opportunity to respond to Patent Owner's new declaration, which was not part of the record of IPR2020-01421. *See* Exs. 1042, 1043. Given Patent Owner's suggestion that such a combination may be possible (i.e. what could have been done) (Prelim. Resp. 30), even if beyond the skill of an ordinary artisan, we decline to deny institution based on the alleged problems with achieving the combination at this stage.[8]

Patent Owner also argues "Ellsberry and Jeddeloh are directed to different problems in the art." Prelim. Resp. 11. Specifically, Patent Owner argues "Ellsberry is directed to a distributed memory architecture and is exclusively focused on expanding a memory module's capacity by using multiple ranks of memory devices and activating and deactivating the memory devices in real time" and "Jeddeloh is directed to a memory module with a central hub architecture with a separate self-test module that is not directly connected with the memory devices." *Id.* at 11–12. Patent Owner also asserts "[t]here is no other problem that Ellsberry seeks to resolve,

[8] Patent Owner asserts that, unlike IPR2020-01421, Patent Owner "provides new evidence to rebut those arguments, supported by expert declaration testimony." Prelim. Resp. 20 n.4. Although Patent Owner presents some new arguments (especially regarding production testing), we did not determine that the new arguments undermined Petitioner's contentions sufficiently. Additionally, to the extent that Patent Owner's declarant repeated arguments presented in the prior preliminary response in IPR2020-01421, further explanation of those arguments rather than just repetition of the arguments would have been helpful.

indeed, Ellsberry makes no mention of any need or desire to implement any form of testing on the memory module for any purpose." *Id.* at 12 (citing Ex. 1005; Ex. 2001, ¶¶ 40, 30). Finally, Patent Owner asserts, "[i]n sharp contrast, the '523 Patent and the challenged claims are directed to system integration and initialization—i.e., to testing during standard operation of the device—and include a 'first mode' or normal mode in which the module operates as normal within a computer system, such as a personal computer system," which according to Patent Owner "is a completely different type of 'testing' than disclosed in Jeddeloh." *Id.* at 13.

As an initial matter, the distinction between testing in Jeddeloh and the '523 patent may be relevant to whether Jeddeloh is analogous art, but Patent Owner does not present an analogous art argument. *See id.* at 13–14.

Additionally, as to whether Ellsberry and Jeddeloh are designed to serve completely different purposes from one another, it is not correct, as Patent Owner suggests, "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem." *KSR*, 550 U.S. at 1742. To the contrary, the Court in *KSR* explained, "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id.* An ordinarily skilled artisan may be motivated to pursue the desirable properties taught by one prior art reference, even if that means foregoing the benefits taught by another prior art reference. *See In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016); *see also Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("[A] given course of

action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine."). Thus, this argument does not sufficiently undermine Petitioner's contentions.

Patent Owner also argues Petitioner's specific motivations to add self-test to Ellsberry, i.e. Reason for Testing, are insufficient. Patent Owner argues, as to Petitioner's first argument, Petitioner's reliance on the statement that "[a]s chips become faster in frequency, there is a greater need for hardware to include self-test logic" (Pet. 32) fails on the basis that "just because a device has a fast clock speed does not mean a BIST must be included *on the module itself*" and "just because Bravo may have found it advantageous to add self-test logic on a relatively simple system would not have meant a POSITA would have believed it to be advantageous to add the same logic on a complex, distributed system like Ellsberry." Prelim. Resp. 15–16. However, the statement of motivation relied on by Petitioner applies more widely than Patent Owner's limited view. Thus, this argument does not sufficiently undermine Petitioner's contentions.

Patent Owner also argues, as to Petitioner's third argument, that Petitioner's reliance on the fact that the purpose of testing is to confirm the module would operate appropriately in normal mode (Pet. 31) fails because "Petitioner's argument ignores the fact that Jeddeloh's disclosure is in the context of *production* testing, which is different from the system integration operational testing disclosed in the claims of the '523 Patent." *Id*. at 12, 13, 17. We note that Patent Owner's declarant states that "[t]he claims of the '523 Patent . . . are directed to . . . testing, during operation once the module has been integrated into an end-computer system." Ex. 2001 ¶ 26. However, Petitioner's declarant does not provide further support or

explanation for this statement. Additionally, Patent Owner's citations to Ex. 1001, 7:36–39, 13:59–62 and claim 1 do not sufficiently support the contention that the '523 Patent is limited to production testing. Additionally, Petitioner has not had the opportunity to respond to this distinction. Although this issue may be shown to have some merit, at this stage, we decline to discount Petitioner's reliance on the statements in Jeddeloh to provide motivation to combine based on this argument.

Patent Owner also asserts "the proposed combination put forward by Petitioner actually has the potential to *increase* signal timing issues, vitiating Petitioner's proposed motivation to combine." Prelim. Resp. 17. We further determine that even if timing issues are increased, a person of ordinary skill can weigh the benefits of testing against the timing issues created. *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349, n.8 (Fed. Cir. 2000) (competing benefits do not weigh against obviousness, rather, the benefits, both lost and gained, in combining the teachings of the prior art should be weighed against one another). Therefore, this argument does not sufficiently undermine Petitioner's contentions.

"There is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention. Rather, the suggestion to combine may come from the prior art, as filtered through the knowledge of one skilled in the art." *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1361 (Fed. Cir. 2006) (citation omitted). The need for self-test in faster chips and the need for self-test to confirm the operation of normal mode in chips is something one of ordinary skill can take into account, even if Jeddeloh and Ellsberry are not specifically included in the support upon which Petitioner relies.

We generally agree, however, with Patent Owner's arguments that: 1) as to Petitioner's first argument, Ellsberry's mention of JEDEC compliance is not specific to self-test; 2) as to Petitioner's second and fourth argument, that Ellsberry's silence as to self-test does not suggest adding self-test; 3) and also as to Petitioner's fifth and sixth argument, that the existence of a "Mode" does not provide motivation to add any and all modes. Prelim. Resp. 14, 17–18.

Patent Owner further argues that each of Petitioner's motivations fails because Petitioner is relying on hindsight. *Id.* at 20. Because we are persuaded, at this stage of the proceeding, by some of Petitioner's proposed bases of motivations, we do not agree that Petitioner is relying on hindsight.

Patent Owner also argues that there are some instances of teaching away in the record. Prelim. Resp. 21–25, 33–40. A teaching away requires a reference to actually criticize, discredit, or otherwise discourage the claimed solution. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004) ("The prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed.").

More specifically, Patent Owner argues Petitioner's "insertion of the MUX/DEMUX into the data paths in Ellsberry's memory bank switches" is "exactly what Ellsberry is designed to avoid." Prelim. Resp. 33. Patent Owner relies on the '901 patent, which is incorporated by reference in the '523 patent, which states

> the multiplexer and/or demultiplexer 12 can present transmission line discontinuity regions in electronic systems (e.g., in electronic systems with signal paths with electrical

> lengths longer than ¼ of the wavelength of the operational frequency or the signal transition rate). In such systems, signal reflections may occur, changing wave characteristics and degrading system performance. These signal reflections may cause signal distortions and signal integrity issues which can contribute to reduced system performance and eventual failure of the system, thereby limiting the effectiveness of the multiplexer and/or demultiplexer in addressing the signal integrity and power dissipation issues.

Id. at 33–34 (quoting Ex. 2002, 1:44–56). Patent Owner further asserts this is "why Jeddeloh placed its self-test module behind its memory interfaces 270a-d. It is also exactly why Ellsberry chose to avoid using FET switches (e.g., MUX/DEMUX) to choose between two different banks of its memory devices." *Id.* at 34. We agree the '901 patent language may appear to disparage the use of multiplexers in certain situations; however, the linkage between the '901 patent statement and the configurations in Ellsberry and Jeddeloh is not sufficiently explained at this stage of the proceeding. We invite additional briefing to address this issue during trial. Additionally, the '901 patent statement uses permissive language such as "may cause" which suggest that, although such a configuration may have been disfavored, it may have been a viable option. Merely teaching an alternative or equivalent method does not teach away from the use of a claimed method. *See In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) (citations omitted); *In re Dunn*, 349 F.2d 433, 438 (CCPA 1965).

Patent Owner additionally asserts that "Ellsberry went to great lengths to design two approaches of activating/deactivating the memory banks 'depending on two different memory addressing schemes (e.g., column or row addressing).'" Prelim. Resp. at 34. Specifically, Patent Owner argues "[t]his was done to avoid the need to control the data paths using any

hardwired switching mechanisms." *Id.* (citing Ex. 1005 ¶ 33; Ex. 2001 ¶ 48). In fact, in the background of the invention, as quoted by Patent Owner, Ellsberry warns when

> [a] high-speed switching system, field effect transistor (FET) switches, is employed to select a data line associated with each level of a stacked memory module to reduce the loading effect on the data lines in memory access. The problem with this scheme is that while FET switches have a fast propagation delay, their switch time is too slow and imprecise to reliably comply with industry standards, such as the Joint Engineering Device Engineering Council (JEDEC) standards, used in many memory applications.

Ex. 1005 ¶ 9.

Nevertheless, Petitioner asserts "[a] Skilled Artisan would have understood that the bidirectional drivers 402 and 404 perform a multiplexing/demultiplexing function depending on the direction of driving. EX1003, ¶¶110-111. It is this use of bidirectional drivers which solve the problem of the prior-art FET switches described in the background of Ellsberry. *Id*." Pet. 18 n.2. In other words, Petitioner suggests "multiplexing/demultiplexing function[s]" are in fact contemplated by Ellsbury. Patent Owner suggests that any multiplexer would be a type of FET Switch. Prelim. Resp. 34 (citing Ex. 2001 ¶¶ 47–48). Patent Owner also suggests JEDEC standards compliance is a reason that would prevent a person of ordinary skill from pursuing this combination. *Id.* For similar reasons as above, Patent Owner also suggests such a combination would be

beyond the ability of one of ordinary skill to have a reasonable expectation of success in achieving.[9] *Id.* at 36–40.

As to this complex technology, and at this juncture, we considered and credited Dr. Subramanian's testimony regarding the feasibility of combination as well as Dr. Brogioli's testimony regarding the unfeasibility of combination at this juncture. Ex. 1003 ¶ 242; *see also Wyers*, 616 F.3d at 1240 n.5 (Fed. Cir. 2010) ("expert testimony may be critical, for example, to establish … the existence (or lack thereof) of a motivation to combine references"). Although Petitioner has provided sufficient evidence in support of its assertions, we cannot fully resolve this conflict between the parties' characterization of multiplexing functions at this stage and on this record. Again, we invite additional briefing on any linkage between the problem asserted in the background of the invention and the two alleged solutions.

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[9] Patent Owner uses the term undue experimentation. Prelim. Resp. 36. Undue experimentation is part of the enablement inquiry. *See Impax Labs., Inc. v. Aventis Pharms. Inc.*, 545 F.3d 1312, 1314 (Fed. Cir. 2008) ("[A] prior art reference must enable one of ordinary skill in the art to make the invention without undue experimentation."). A reference, however, qualifies as prior art in determining obviousness, independent of enablement. *In re Antor Media Corp.*, 689 F.3d 1282, 1292 (Fed. Cir. 2012); *see also In re Morsa*, 713 F.3d 104, 111–12 (Fed. Cir. 2013) (remanding for proper enablement analysis in anticipation rejection, but affirming obviousness rejection based on the same prior art). Thus, we do not engage in enablement analyses in our obviousness determination. Instead, we interpret Patent Owner's undue-experimentation argument as an assertion of no reasonable expectation of success.

Thus, for the reasons above, for purposes of this decision, and based on Petitioner's citations to specific prior art disclosures and supporting evidence, we are persuaded that Petitioner sets forth sufficient articulated reasoning with rational underpinning to support the legal conclusion that it would have been obvious to modify the teachings of Ellsberry with Jeddeloh's teachings to include self-test functionality. Pet. 31–37.

a. Independent claim 1

i. Limitation [a] (Preamble)

Petitioner contends that Ellsberry teaches a memory module accessible in a computer system by a system memory controller via a system memory bus, as recited in the preamble of claim 1. Pet. 38. Petitioner relies upon Ellsberry's disclosure of "memory module 106," "processing unit 102," that is "coupled to a memory module 106 to retain or store information," and that Ellsberry's memory module is accessible by the memory controller "*via a system memory bus*" as reflected by path 110 (Figure 1), corresponding DIMM interface with data buses 230–232 (Figure 2), and corresponding edge interface (Figures 5 and 6). *Id.* (citing Ex. 1005 ¶¶ 11, 17, 23, 26–28, 47, 51, Figs. 1, 2, 5, 6; Ex. 1015, 6; Ex. 1003 ¶¶ 171–175).

We have reviewed the record, and find that Petitioner provides sufficient evidence that the prior art teaches the preamble and limitation [a] of claim 1.[10] Patent Owner makes no arguments contesting the prior art teachings of these claim limitations. *See generally* Prelim. Resp.

[10] We need not determine whether the preamble of claim 1 is limiting because Petitioner has sufficiently shown that the combination of Ellsberry and Jeddeloh teaches the preamble at this juncture. *See Nidec*, 868 F.3d at 1017.

ii. Limitation [b]

Petitioner contends that limitation [b] of claim 1 is taught by Ellsberry's disclosure DRAMs which are mounted on a circuit board. Pet. 38–39 (citing Ex. 1005 ¶¶ 3, 30, 32, 47, 49, 51, 54, 56, Figs 5, 6, 11, 13; Ex. 1003 ¶ 180). Petitioner contends that Ellsberry discloses "*address and control ports*" and "*data ports*" coupled to the address and control lines from the Control ASICs (ACA/ACB/ACAA/ACBB, CS0A-CS1BB) and data lines from the Switch ASIC (DQA/DQB), respectively. *Id.* at 39–40 (citing Ex. 1005 ¶ 30; Ex. 1003 ¶¶ 181–82).

We have reviewed the record, and find that Petitioner provides sufficient evidence that Ellberry teaches limitation 1[b]. Patent Owner makes no other arguments contesting the prior art teachings of this claim limitation. *See generally* Prelim. Resp.

iii. Limitation [c]

Petitioner asserts that Ellsberry's nine Switch ASICs ("D") in Figures 5 and 6 collectively comprise "*a data module*," correspond to Switch ASICs 206-208 (Figure 2) (mounted on a circuit board), and pass data between the memory devices and the memory bus/memory controller. Pet. 40–42 (citing Ex. 1005 ¶¶ 3, 28–30, 47, 49, 51, Fig. 2; Ex. 1003 ¶¶ 186–87). Petitioner further contends that Ellsberry's Switch ASICs are "*coupled between the data ports of the memory devices and the system memory bus*" because Figure 2 shows them coupled between DIMM interface 202 and the "*data ports of the memory devices*" (212–228). *Id.* at 42 (citing Ex. 1005 ¶¶ 11, 28–30, 47, Figs. 5, 6, 11, 13; Ex. 1015, 6; Ex. 1003 ¶ 188). Petitioner contends Ellsberry's "*data module*" (Switch ASICs) in all embodiments "*includ[es] data handler logic elements*" located in the "control block" of

Figure 4 and, in the combined system, the "*data handler logic elements*" would also include logic elements implementing the functionality of Jeddeloh's pattern generator and compare circuitry. *Id.* at 42–43 (citing Ex. 1005 ¶ 45; Ex. 1006, 9:44–10:67; Ex. 1003 ¶¶ 136–165, 190).

We have reviewed the record, and find that Petitioner provides sufficient evidence that Ellsberry teaches limitation 1[c]. Patent Owner makes no arguments contesting the prior art teachings of this claim limitation. *See generally* Prelim. Resp.

iv. Limitation [d]

Petitioner contends that Ellsberry teaches limitation [d] by its disclosure of a Control ASIC ("*control module*"), that is "*coupled to the data module*" (Switch ASICs) via bus 210, "*coupled to… the address and control ports of the memory devices*" via bus 220, as depicted in greater detail in, and "*coupled to… the system memory bus*" via DIMM interface 202 (Figure 2), corresponding to the edge interface of Figure 5 and 6. Pet. 44 (citing Ex. 1005 ¶¶ 28–32, 47–52, 54, 56, Fig. 11, 13; Ex. 1015, 6; Ex. 1003 ¶¶ 194–99). Petitioner further contends that in the First Embodiment,[11] the "*control module*" is depicted in Figure 5 as "C" and in Figure 13 as Control Unit ASIC 1302 and in the Second Embodiment, the "*control module*" comprises two "control units 604" (individually or collectively) with one depicted as "C" in Figure 6 and shown in Figure 11 as Control Unit ASICs 1102/1104 and as depicted in Figures 5 and 6, the Control ASIC(s) is/are

[11] Petitioner asserts "FIGS. 2, 5, and 13 of Ellsberry correspond to a 'First Embodiment' utilizing four ranks, each composed of nine 8-bit memory devices for a total bit width of 72. FIGS. 2, 6, and 11 correspond to a 'Second Embodiment' utilizing pairs of 4-bit memory devices to implement the same bit width. EX1003, ¶108." Pet. 22.

"*mounted on the circuit board*." *Id.* at 45–46 (citing Ex. 1005 ¶¶ 3, 47, 49, 51, Figs. 5, 6; 1003 ¶¶ 194–95).

We have reviewed the record, and find that Petitioner provides sufficient evidence that Ellsberry teaches limitation 1[d]. Patent Owner makes no arguments contesting the prior art teachings of this claim element. *See generally* Prelim. Resp.

v. Limitation [e]

Petitioner asserts that the combination of Ellsberry and Jeddeloh teaches limitation 1[e] by Ellsberry's disclosure of a normal mode used to read/write DRAMs in response to controller commands and, in the proposed combination, by Ellsberry operating in a test mode as taught by Jeddeloh. Pet. 46–48 (citing Ex. 1005 ¶¶ 41, 42, Fig. 8A; Ex. 1003 ¶¶ 203–10).

We have reviewed the record and find that Petitioner provides sufficient evidence that the combination of Ellsberry and Jeddeloh teaches limitation 1[e]. Patent Owner makes no arguments contesting the prior art teachings of this claim limitation. *See generally* Prelim. Resp.

vi. Limitation [f.i]

Petitioner contends that Ellsberry teaches limitation [f.i] by its disclosure Control ASIC ("*control module*"), in the first (normal) mode, "*receive[s] system address and control signals from the system memory controller*" over the DIMM interface (Figure 2), which corresponds to the edge interface of Figures 5 and 6. Pet. 48–49 (citing Ex. 1005 ¶¶ 29, 35, 36, 45, 47, 51, Figs. 2, 5, 6, 8A, 11, 13, code (57); Ex. 1003 ¶¶ 168–77, 193–201, 218). Petitioner also contends the Control ASIC in the first mode is also configured to output address and command signals ("*first memory address and control signals*") to the memory devices on bus 220 according

to the received system signals, for example, in Figures 3, 11, and 13. *Id.* at 45. Additionally, Petitioner contends Ellsberry also lists "*first memory address and control signals"* in Figure 8A, such as READ/WRITE/NOP, and describes operations relating thereto. *Id.* at 50–51 (Ex. 1005 ¶¶ 10, 11, 33, 41, 42, Figs. 8A, 11, 13; Ex. 1003 ¶ 219).

We have reviewed the record, and find that Petitioner provides sufficient evidence that Ellsberry teaches limitation 1[f.i]. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

vii. Limitation [f.ii]

Petitioner contends that Ellsberry teaches limitation [f.ii] by its disclosure of, in Figure 2, Switch ASICs ("*data module*") that "*propagate*" 8-bit sections of "*first data signals*" between "*the memory devices*" (DRAM) and DIMM interface (which is connected to "*the system memory controller*") via 8-bit buses (green), and, in Figure 4, details of the Switch ASIC bus connections. Pet. 52 (citing Ex. 1005 ¶¶ 29–30, 45; Ex. 1003 ¶¶ 168–177, 185–192). Petitioner further contends that Figures 5 and 13, as well as 6 and 11, contain corresponding depictions of Switch ASICs that "*propagate*" respective 8-bit sections of 72-bit wide "*data signals between the memory devices and the system memory controller,*" with Figures 5 and 6 each showing nine switch ASICs coupled between an edge interface (corresponding to DIMM interface) and four sets of nine 8-bit DRAMs (504 & 512) or pairs of 4-bit DRAMs, and Figure 13 showing each Switch ASIC in Figure 5 receives 8-bit signals from the system memory controller (DQ) and passes it to one of four DRAMs via 8-bit signal lines (DQA/DQB), and with Figure 11 functioning like Figure 13, but utilizing pairs of 4-bit

DRAMs instead of single 8-bit DRAMs, and two Control ASICs instead of one. *Id.* at 52–55 (Ex. 1005 ¶¶ 2, 47–51; Ex. 1003 ¶¶ 99–104, 226–232).

We have reviewed the record, and find that Petitioner provides sufficient evidence that Ellsberry teaches limitation 1[f.ii]. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

viii. Limitation [f.iii]

Petitioner contends that Ellsberry teaches limitation [f.iii] by its disclosure of "*first data signals*" are "*transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals*" such as a write or read command received over bus 220 in Figure 2. Pet. 55–56. In Ellsberry's First and Second Embodiments, for example, the Control ASIC "maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)." *Id.* (citing Ex. 1005 ¶¶ 11, 31, Fig. 2; Ex. 1003 ¶¶ 211–222, 236–237).

Specifically, Petitioner contends that "when row/bank mode addressing is used, read and write commands are sent only to the targeted memory device [and it performs the read/write] … [whereas a] NOP (no-operation) command is sent to the non-targeted memory device," allowing the Control ASIC to "control data to and from" the memory devices "without the delays caused by otherwise disabling" the non-targeted devices and Ellsberry's memory devices receiving a NOP command do not

transmit/receive data because NOP commands are not registered. *Id.* at 56 (Ex. 1005 ¶¶ 33, 42; Ex. 1028, 14; Ex. 1003 ¶¶ 238, 239).

We have reviewed the record, and find that Petitioner provides sufficient evidence that Ellsberry teaches limitation 1[f.iii]. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

ix. Limitation [g.i]

Petitioner contends that the proposed combination teaches limitation [g.i] in that during test mode in the Combined System, the modified Control ASIC ("*control module*") would "*output second memory address and control signals to the address and control ports of the memory devices*," similar to how Ellsberry's Control ASIC outputs address/control signals during normal operation. Pet. 56 (citing Ex. 1006, 9:51–10:2, 10:24–29, Fig. 3; Ex. 1003 ¶¶ 243–50).

We have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry and Jeddeloh teaches limitation 1[g.i]. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

x. Limitation [g.ii]

Petitioner contends that the combined system teaches limitation [g.ii] in that there are two sources of data for the memory devices: (i) the system memory controller (during normal mode) and (ii) the pattern generator/compare circuit functionality in each Switch ASIC (during test mode), thus, each source communicates data along a different path in the Switch ASICs, so that "*the system memory controller*" is "*isolate[d]*" from the "*memory devices*" during test mode ("*second mode*") according to

commands from the Control ASIC ("*control module*"). Pet. 57–60 (citing, *inter alia*, Ex. 1003 ¶ 255–59). Additionally, according to Petitioner, during test mode, the pattern generator functionality of the modified Switch ASICs "*transmit[s] one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices*," similar to how Ellsberry's Switch ASICs transmit data during normal operation. *Id.* at 60–61 (citing, *inter alia*, Ex. 1003 ¶¶ 273–75).

We have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry and Jeddeloh teaches limitation 1[g.ii]. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

xi. Limitation [g.iii]

Petitioner contends that the combined system teaches limitation [g.iii] in that the modified Control ASIC outputs address/control signals ("*second memory address and control signals*") to the ports of the memory devices 240. Pet. 61 (citing Ex. 1006, 9:51–56, 9:56–60, 9:66–10:2, cl. 7, Fig. 3; Ex. 1003, 279–80).

For example, Petitioner contends Jeddeloh's memory sequencer 304 "generates properly timed signals for controlling the operation of the memory devices 240" as shown in Figure 2 (Ex. 1006, 9:57–60), "the self-test module 300 can also vary the timing and rate at which control and address signals are applied to the memory devices 240 along with the CLK signal or other timing signal" (*id.*, 10:24–28), and Figure 3 further shows a "RD/WRT" signal from the BIST engine 310 to the memory sequencer 304, confirming that signals output from memory sequencer 304 during testing include signals for the memory devices, sent via Ellsberry's bus 220 in the

combined system, to configure them to receive test data ("*second data signals*") (*id.*, Fig. 3). Pet. 61 (citing Ex. 1003 ¶¶ 279–80).

We have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry and Jeddeloh teaches limitation 1[g.iii]. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

xii. Conclusion

On this record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claim 1 would have been obvious over Ellsberry.

c. Independent Claim 19

Independent claim 19 is an apparatus claim with limitations that parallel most of those in claim 1. *Compare* Ex. 1001, 16:54–17:30 *with id.* at 19:4–43. Petitioner additionally contends that the "*PCB*" of claim 19 is equivalent to Ellsberry's "substrate 502," and the "*connector*" is equivalent to Ellsberry's DIMM interface and edge interface. Pet. 92–97 (citing Ex. 1005 ¶¶ 2, 11, 27, 28, 47, 51, Figs. 1, 2, 5, 6, 11, 13; Ex. 1015, 6, 29, 66; Ex. 1003 ¶¶ 168–241, 254, 282–333, 348–53, 354–62, 365–71, 428–31, 467–85, 540–45, 548–53, 555–57, 560, 562–66, 568–71). Petitioner asserts that, as applied in element [1.f.ii], Ellsberry's system memory controller connects to the memory module via Ellsberry's DIMM interface (Figure 2) ("*connector*")/edge interface (Figures 5 and 6) ("*connector*") for "*read or write operations*" over the bidirectional data signal lines to each Switch ASIC ("*data handlers*") shown in Figures 2 and 4. *Id.* at 95–96 (Ex. 1003 ¶¶ 564–566).

We have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry and Jeddeloh teaches the limitations of claim 19. Patent Owner makes no arguments contesting the prior art teachings of the limitations of this claim. *See generally* Prelim. Resp.

On this record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claim 19 would have been obvious over the combination of Ellsberry and Jeddeloh.

e. Dependent Claims 2–18, 20–34

Petitioner asserts that the combination of Ellsberry and Jeddeloh teaches the limitations of dependent claims 2–18 and 20–34. Pet. 62–93, 97–104. We have reviewed the record and find that Petitioner provides sufficient evidence that the combination of Ellsberry and Jeddeloh teaches the limitations of these dependent claims. Patent Owner makes no arguments contesting the prior art teachings of the limitations of these claims. *See generally* Prelim. Resp.

On this record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claims 2–18 and 20–34 would have been obvious over the combination of Ellsberry and Jeddeloh.

E. Alleged Obviousness of Claims 1–34 Over Ellsberry, Jeddeloh, and Averbuj

Petitioner contends that claims 1–34 would have been obvious over the combination of Ellsberry, Jeddeloh, and Averbuj. Pet. 104–10. To support its contentions, Petitioner provides explanations as to how Ellsberry, Jeddeloh, and Averbuj teach each claim limitation. *Id.*

Averbuj (Ex. 1007) "is directed to a distributed, hierarchical built-in self-test (BIST) architecture for" memory modules. Ex. 1007 ¶ 7. Averbuj discloses a memory interface used for self-test functionality. *Id.*, Fig. 6. Multiplexers 45 and 46 in the memory interface 41 are used to merge and select between multiple signal paths. *Id.* ¶ 48. During BIST mode, the memory interface 41 receives test data signals from sequencer 8, and either provides the same data to its memory device as is, or generates its own data by modifying the signals from the sequencer. *Id.* ¶¶ 11, 48–50, 55–56, Figs. 6–7.

Petitioner states that Averbuj is asserted "[t]o the extent [Patent Owner] argues the modified Switch ASICs in test mode do not satisfy that the '*configured to isolate*' limitations of claims 1, 11, 32." Pet. 104. For example, Petitioner contends "Averbuj discloses a modular BIST architecture for memory modules, including a memory interface with two data paths, one from the system memory controller ('programmable processor') for normal operations (green, DATA) and one from a pattern generator during test operations (blue, BIST_DATA_T), to be merged and selected between for provision to the DRAM." Pet. 105. Additionally, Petitioner contends Averbuj discloses using MUX 45 for that purpose, that "isolates" the DRAM "from normal functionality . . . in BIST mode" in response to the BIST_EN command from a sequencer. *Id.*

We determined that the combination of Ellsberry and Jeddeloh were sufficient to show a reasonable likelihood of success as to claim 1–34. We have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry, Jeddeloh, and Averbuj teach the limitations of claims 1–34, and sufficient rationale to combine the prior art

has been provided. Patent Owner presents no issues or arguments specific to the asserted obviousness contentions beyond motivation to combine Ellsberry and Jeddeloh discussed above. *See generally* Prelim. Resp.

On this record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claims 1–34 would have been obvious over the combination of Ellsberry, Jeddeloh, and Averbuj.

F. Alleged Obviousness of Claims 14 and 17–34 Over Ellsberry, Jeddeloh, and Lee

Petitioner contends that claims 14 and 17–34 would have been obvious over the combination of Ellsberry, Jeddeloh, and Lee. Pet. 110–12. To support its contentions, Petitioner provides explanations as to how Ellsberry, Jeddeloh, and Lee teach each claim limitation. *Id.*

Lee (Ex. 1008) discloses "a method of testing a memory module, including receiving a test pattern and an associated input mode." Ex. 1008 ¶ 15, code (57). The test pattern and input mode "may [be] received through a system management bus (SMBUS)." Ex. 1008 ¶¶ 31, 62–63. After receiving the test pattern, a pattern generator in the memory module may either generate a test pattern based on it and the input mode, or output that received test pattern without modification. *Id.* ¶¶ 36–38, 64.

Petitioner asserts Lee "[t]o the extent one argues the Combined System does not satisfy the requirements of claims 14 and 17-18, or element [19.h]'s similar '*based on information output from the control module*' limitation, it also would have been obvious to implement the Combined System in such a manner in further view of Lee." Pet. 110. For example, Petitioner contends Lee discloses techniques of generating test pattern data

based on control module information received off-module over a maintenance bus, such as an SMBUS. Pet. 111 (citing Ex. 1008 ¶¶ 15, 16, 36–38, 41–48, 64, Fig. 3; Ex. 1003 ¶¶ 490, 534, 575;). Patent Owner presents no issues or arguments specific to the asserted obviousness contentions beyond the motivation to combine Ellsberry and Jeddeloh discussed above. *See generally* Prelim. Resp.

We determined that the combination of Ellsberry and Jeddeloh were sufficient to show a reasonable likelihood of success as to claims 14 and 17–34. Further, we have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry, Jeddeloh, and Lee teaches the limitations of claims 14 and 17–34, and sufficient rationale to combine the prior art has been provided. Patent Owner makes no additional arguments contesting the prior art teachings of the limitations of these claims or the rationale to combine as to Ellsberry, Jeddeloh, and Lee. *See generally*, Prelim. Resp.

On this record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claims 1–34 would have been obvious over the combination of Ellsberry, Jeddeloh, and Lee.

G. Alleged Obviousness of Claims 14 and 17–34 Over Ellsberry, Jeddeloh, Averbuj, and Lee

Petitioner contends that claims 14 and 17–34 would have been obvious over the combination of Ellsberry, Jeddeloh, Averbuj, and Lee. Pet. 113. To support its contentions, Petitioner provides explanations as to how Ellsberry, Jeddeloh, Averbuj, and Lee teach each claim limitation. *Id.*

Petitioner contends "[t]he *'configured to isolate*' limitation of claim 1, as incorporated into claims 14 and 17-18, would have been obvious in view

of Averbuj" and "Element [19.h]'s '*not accessed*' limitation would have been obvious in view of Averbuj, . . . and the '*based on information*' limitation would have been obvious in view of Lee," based on the contentions in the other grounds of the Petition. Pet. 113. Patent Owner presents no issues or arguments specific to the asserted obviousness contentions beyond motivation to combine Ellsberry and Jeddeloh discussed above. *See generally* Prelim. Resp.

We determined that the combination of Ellsberry and Jeddeloh were sufficient to show a reasonable likelihood of success as to claim 1–34. Furthermore, we have reviewed the record, and find that Petitioner provides sufficient evidence that the combination of Ellsberry, Jeddeloh, Averbuj, and Lee teach the limitations of claims 14 and 17–34, and sufficient rationale to combine the prior art has been provided. Patent Owner makes no additional arguments contesting the prior art teachings of the limitations of these claims or the rationale to combine as to Ellsberry, Jeddeloh, Averbuj, and Lee. *See generally* Prelim. Resp.

On this record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claims 14 and 17–34 would have been obvious over the combination of Ellsberry, Jeddeloh, Averbuj, and Lee.

IV. CONCLUSION

Based on the arguments and evidence presented in the Petition, the Preliminary Response, Reply, and Sur-Reply and accompanying exhibits, we have determined there is a reasonable likelihood Petitioner would prevail with respect to at least one claim challenged in the Petition. We conclude that the threshold has been met for instituting *inter partes* review, and we

institute on all challenged claims and all grounds. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1354 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018). We have not made a final determination on claim construction or as to the patentability of any of the challenged claims. Our final determination will be based on the record as fully developed during trial.

V. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted as to challenged claims 1–34 of the '523 patent for all grounds raised in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this Order.

IPR2022-00063
Patent 10,217,523 B1

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CERTIFICATE OF SERVICE

I hereby certify that on May 12, 2022, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF, which will send notification of such filing to all registered participants.

I further certify that I caused copies of the foregoing document to be served on May 12, 2022, upon the following in the manner indicated:

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